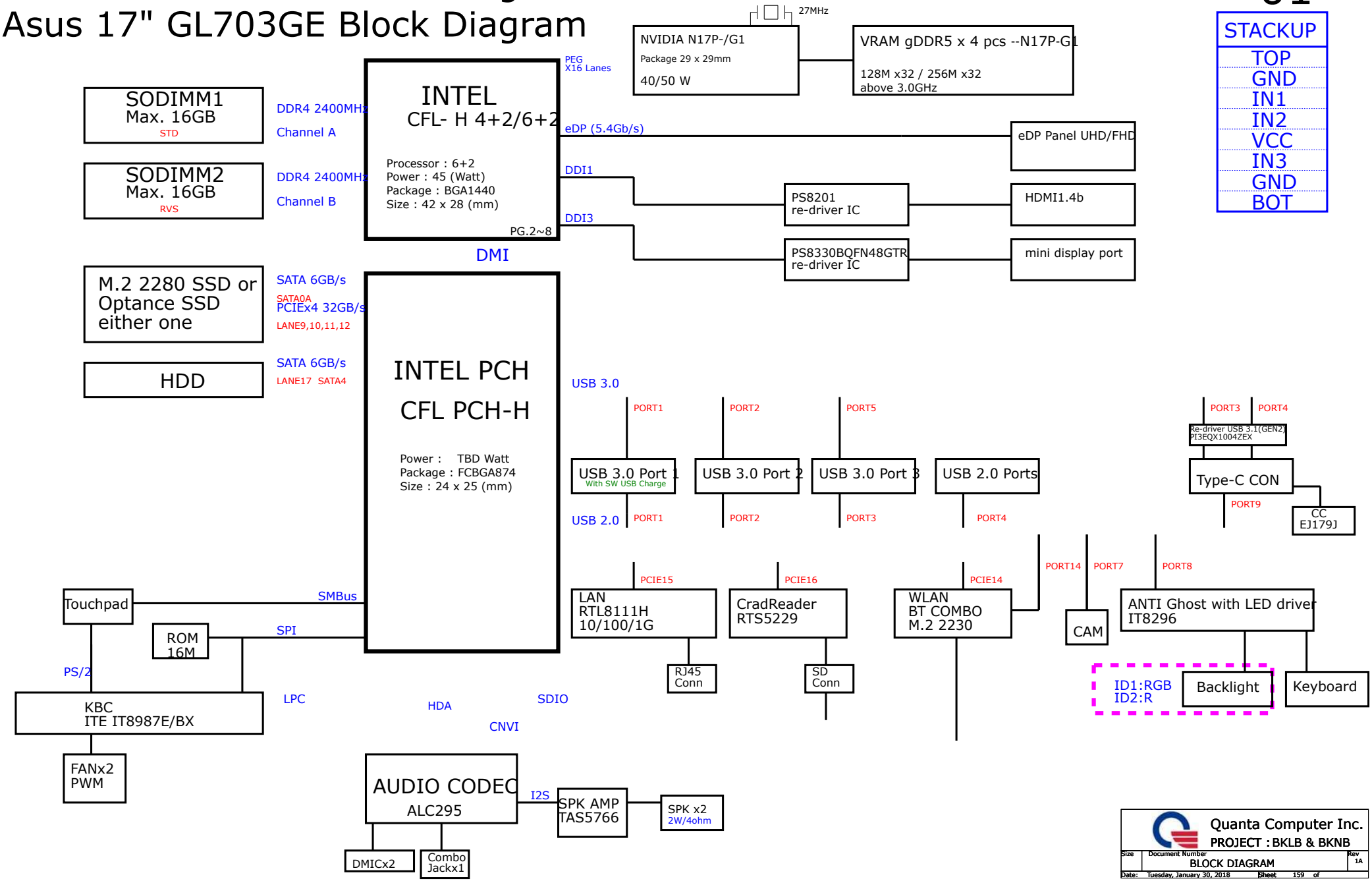
Asus 15" GL503GE Block Diagram
Asus 17" GL703GE Block Diagram

01

STACKUP
TOP
GND
IN1
IN2
VCC
IN3
GND
BOT



Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

Date: Tuesday, January 30, 2018 Sheet 159 of

Model	REV	CHANGE LIST
BKLB BKNB	PR	Page 11 -- Change R1027 pull high from +3V to +3V_S5 for SYS_RESET,Follow CRB request Page 11 -- ADD RTC battery detect for ASSY line request. Page 13 -- ADD R1220 pull high to +3V_S5 for PCH_SPI1_SI and no mount. Page 14 -- ADD GL703GD for 1050 MBID. Page 16 -- DEL R1181,R1179,R1182,R1180,R1183,R1184 Series for PCH SD signal for EMI verify Page 17 -- Modify H12 layout for Thermal issue and add 0ohm for EMI request Page 23 -- Change VR67 from 100K to 150K for solve power off timing for GPU Page 23 -- Add VR174,VQ15,VC486 for solve power off timing for GPU. Re-work ok and verify on latest report Page 23 -- Add VR173,VQ14,VC485 for solve power off timing for GPU. Re-work ok and verify on latest report Page 32 -- Change C320 ,C338,C339 size from 0201 to 0402 for SMT line request. Page 34 -- Change R231 10K from mount to no mount. There is pull high on PCH side. Page 34 -- Change TR3 from 10K to 18.7K. To define GPU thermal OT on 120 degree. Page 35 -- Add AR126 and AR127 Bead for solve ESD and Change AC45 AC42 from 100p to 680P And Change TVS on SLEEVE and RING2 Page 36 -- Add RTC_DET# at GPA0 for Assy line request. Page 36 -- Change KR72 form 100K to 200K for PR stage. Page 50 -- Change KC85 size form 0201 to 0402 for SMT line request. Page 51 -- Add MR28 10K to pull down on PCIE_CLKREQ_CR#, Realtek request to alwayes pull down.
	MP	

DOC NO.	PROJECT MODEL :	BKLB/BKNB	APPROVED BY:		DATE:	2018/01/29
	PART NUMBER:		DRAWING BY:		REVISON:	3A

Quanta Computer Inc.
PROJECT : BKLB & BKNB
Size | Document Number: POWER UP SEQUENCE | Rev: 1A
Date: Tuesday, January 30, 2018 Sheet 259 of

KABY LAKE Processor (CLK,MISC,JTAG)

03

Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impendence 85 ohm

Please remove to CPU side

PROCHOT# (50ohm)
Trace Length <11 inches

Close to U1

Mount 220P for ESD

CPU CORE SVID

Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.

PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE

Close to CPU

SVID CLK

CLOSE TO CPU
PLACE THE PU RESISTORS

SVID ALERT

CLOSE TO CPU
PLACE THE PU RESISTORS

SVID DATA

Placement close to CPU.

For DCI debug

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

0 Enable; SET DFX ENABLED BIT IN DEBUG
1 , Disable;

Mark eDP mode Enabled

Mark PCIE port reserved
N17P used port 8~15

Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

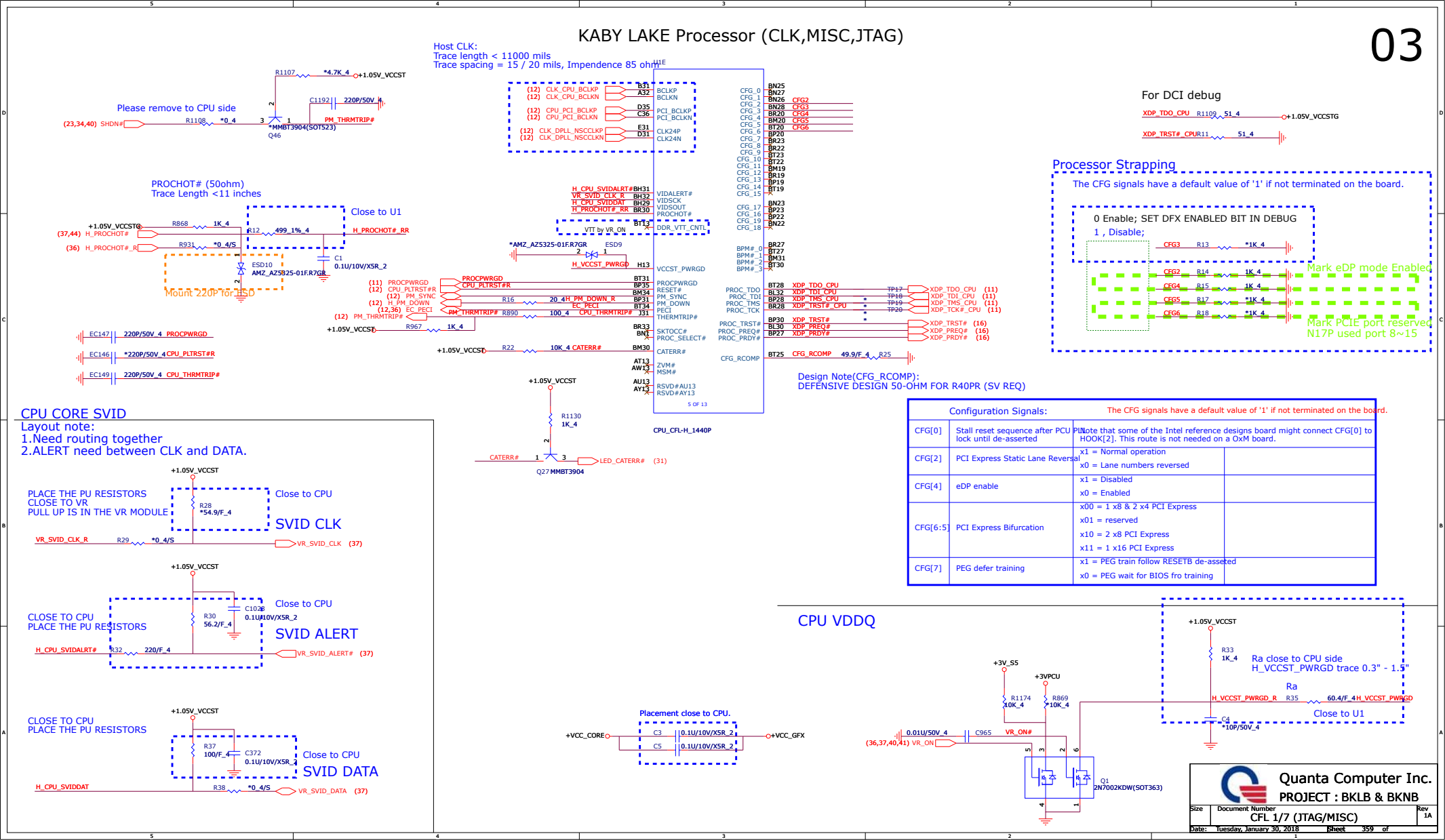
Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a OxM board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asseted x0 = PEG wait for BIOS fro training	

CPU VDDQ

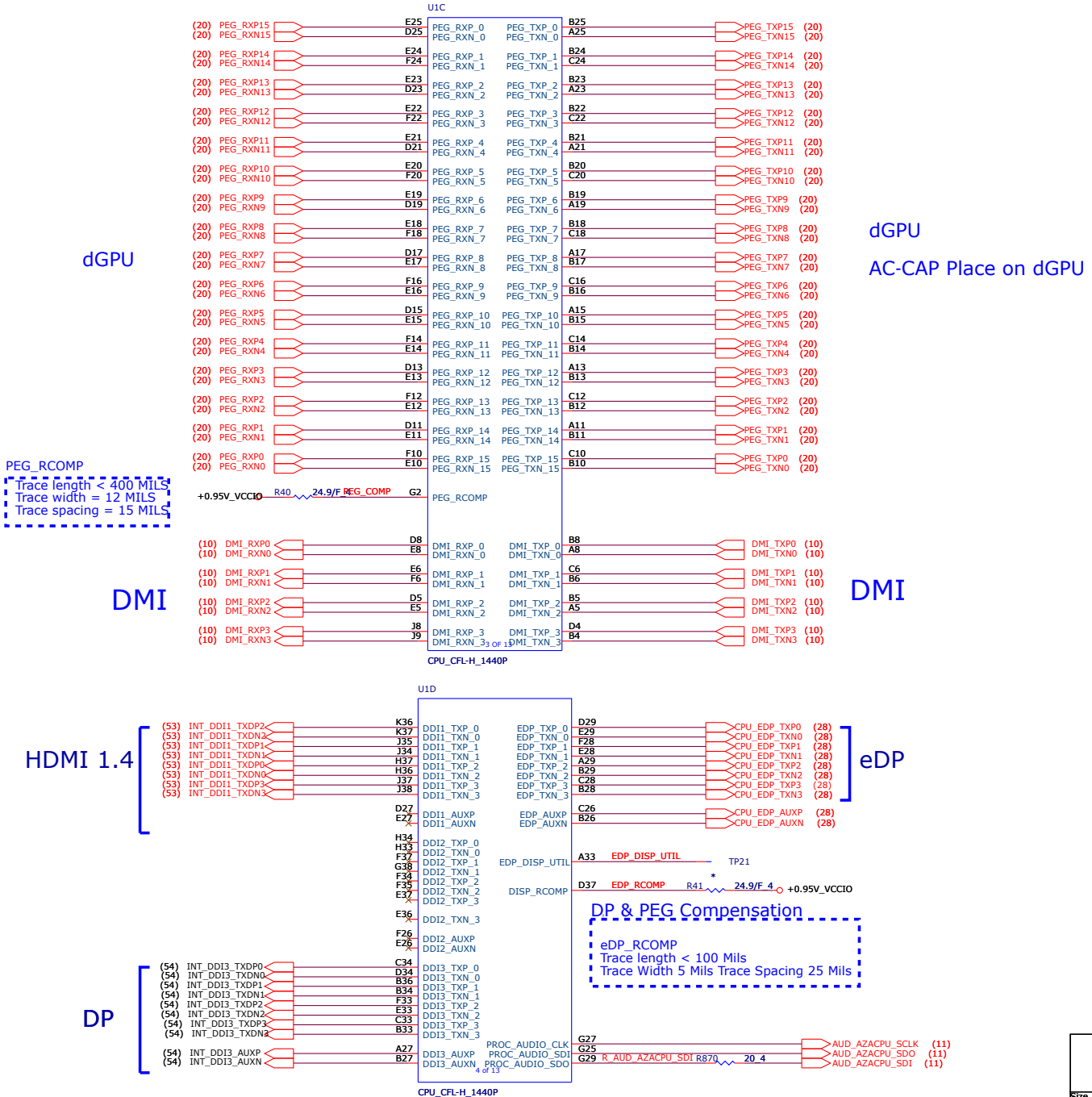
Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"

Ra

Close to U1



KABY LAKE Processor (DMI,PEG,FDI)



Quanta Computer Inc.		
PROJECT : BKLB & BKNB		
Size	Document Number	Rev
	CFL 2/7 (DMI/EDP/PEG)	1A
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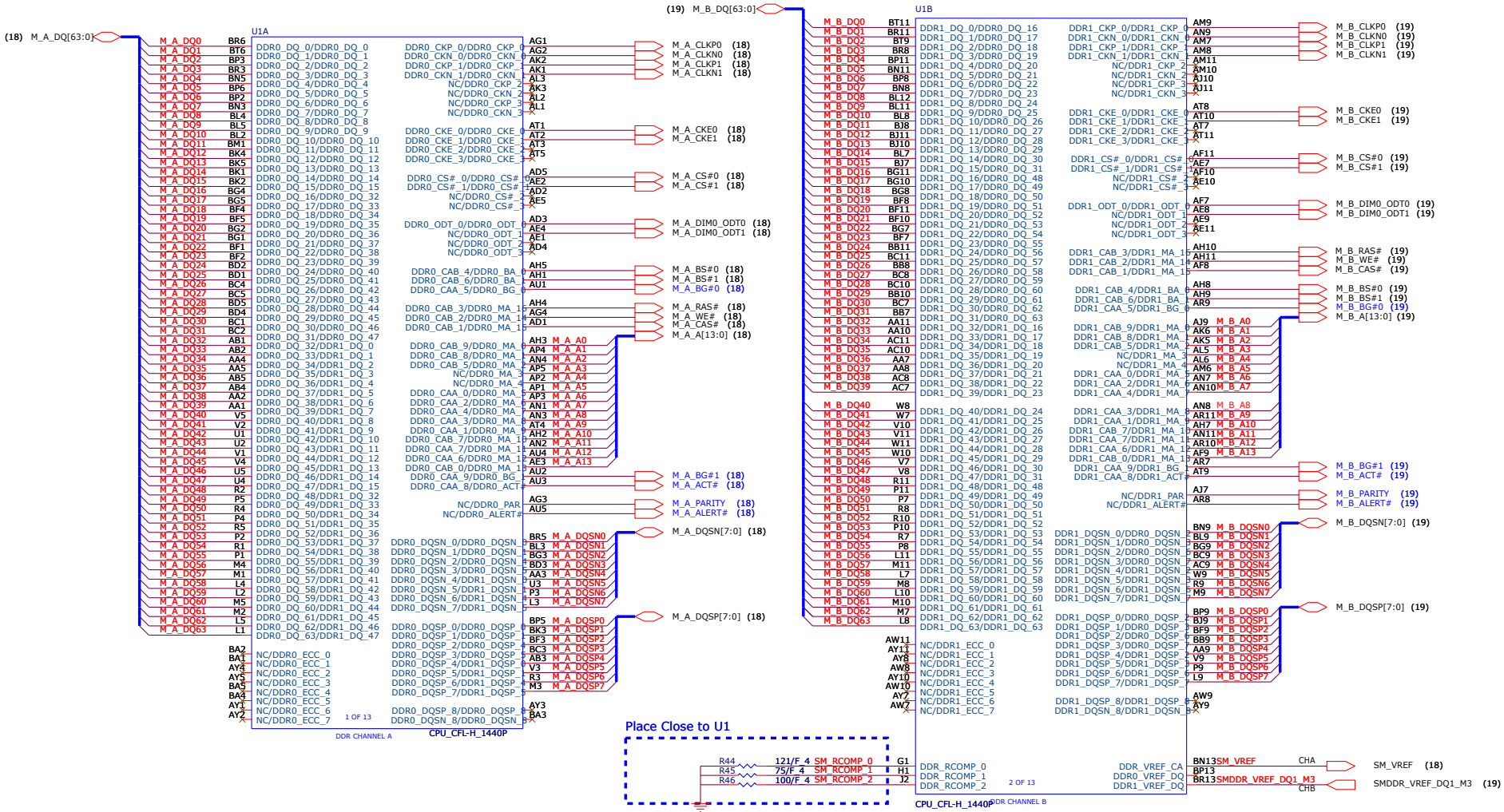
KABY LAKE Processor (DDR4)



Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	CFL 3/7 (DDR4 I/F)	1A

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CFL Processor (POWER)

Follow CFL H page 126 to 45W(GT2): +VCCGT=34A

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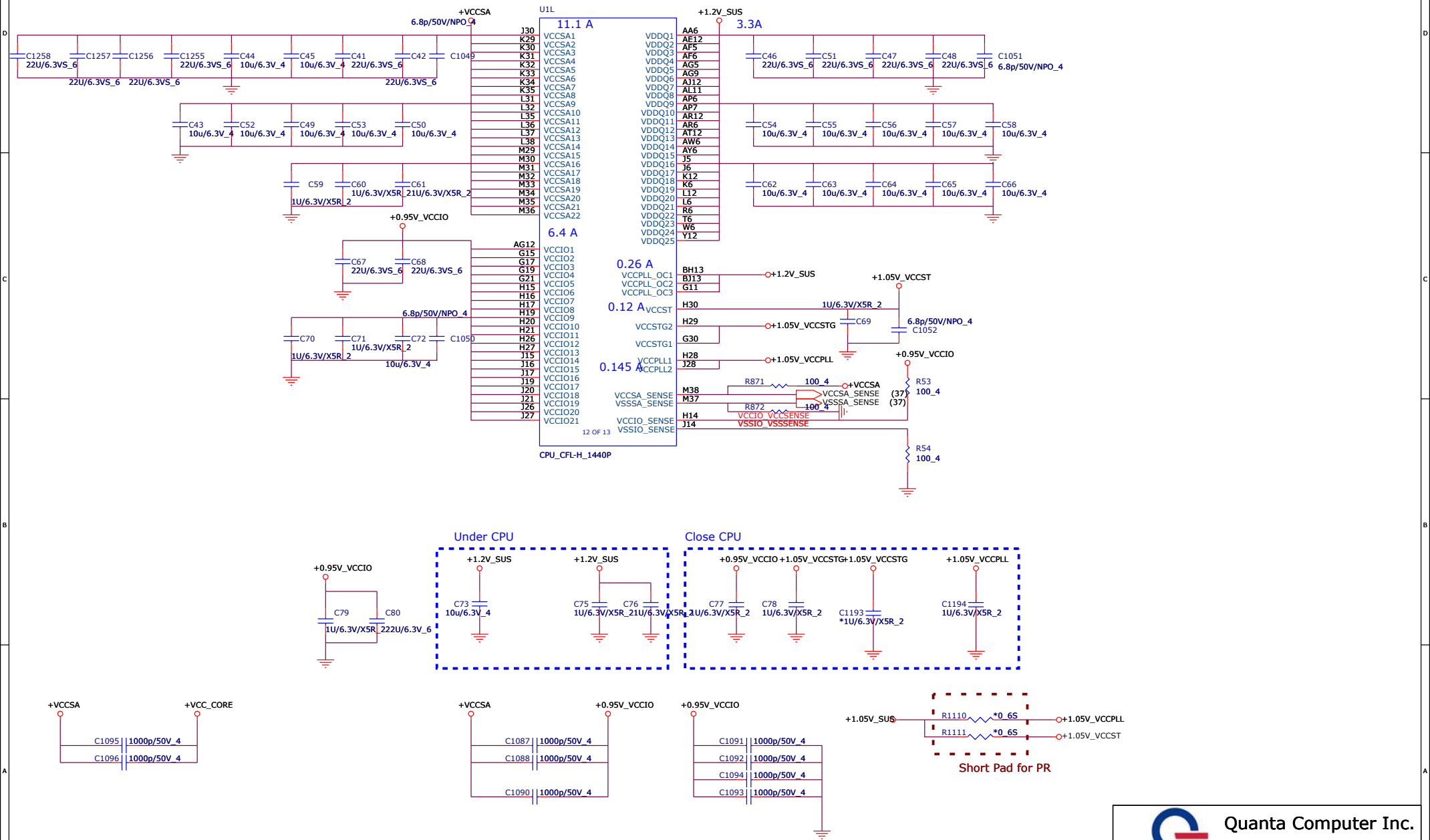
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	CFL 4/7 (POWER)	2A

Date: Tuesday, January 30, 2018 Sheet 659 of



Quanta Computer Inc.	
PROJECT : BKLB & BKNB	
Size	Document Number: CFL 5/7 (POWER&GND) — Rev: 2A
Date: Tuesday, January 30, 2018	Sheet 759 of

Follow CFL H EDS page 130 to 45W(GT2): VCC_CORE=128A for 6 code
Follow CFL H EDS page 130 to 45W(GT2): VCC_CORE=86A for 4 code

+VCC_CORE

U1I

CPU_CFL-H_1440P

9 OF 13

VCC_SENSE
VSS_SENSE

AG37 VCC_SENSE
AG38 VSS_SENSE

VCC_SENSE (37)
VSS_SENSE (37)

R65 100_4
R66 100_4

Add 22u and 1u for 6 core CPU

U1J

CPU_CFL-H_1440P

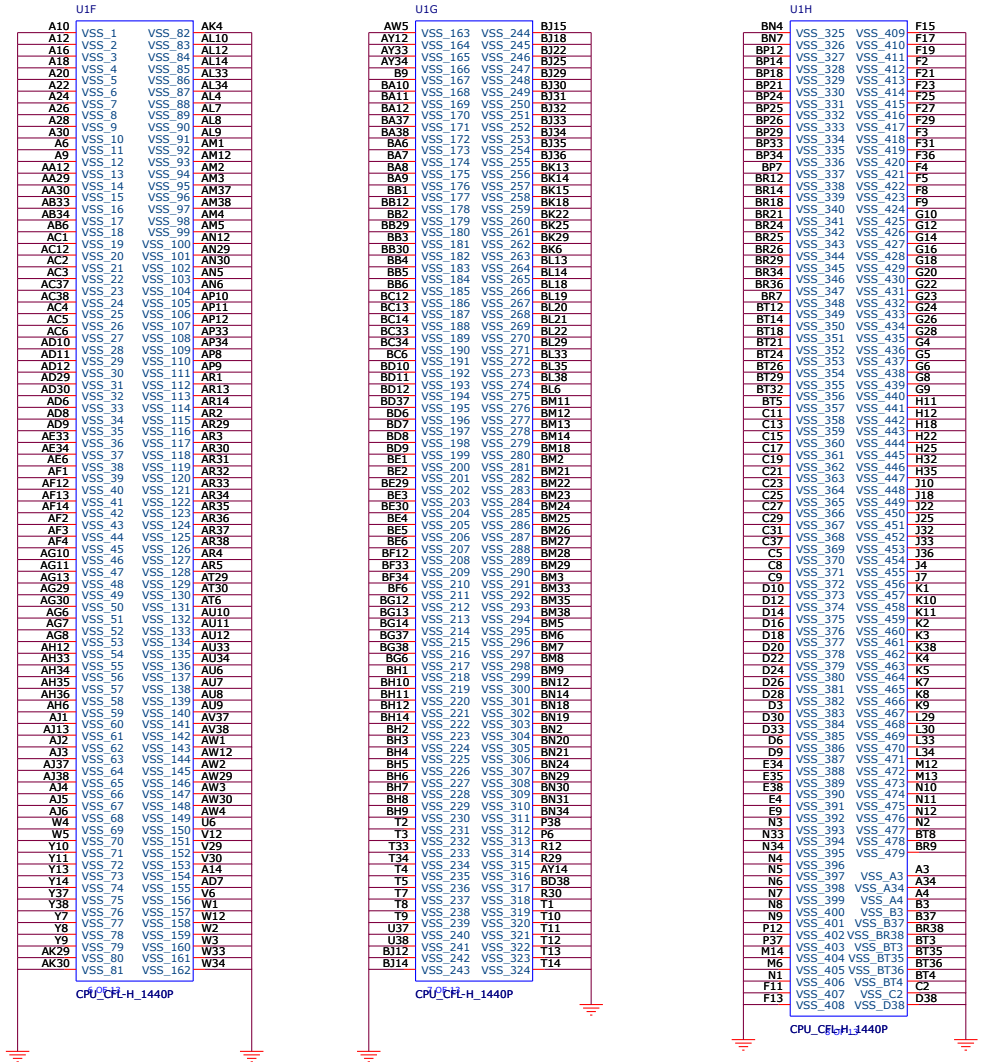
10 OF 13

Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket
Trace Impendence 50 ohm

Quanta Computer Inc.
PROJECT : BKLB & BKNB

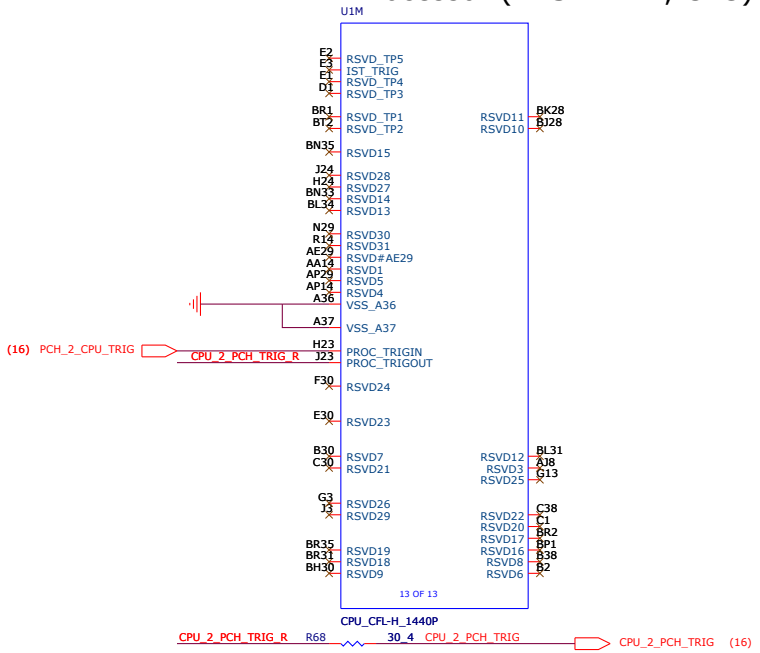
Size	Document Number	Rev
	CFL 6/7 (POWER&GND)	1A
Date: Tuesday, January 30, 2018	Sheet 859 of	

KBL-HProcessor (GND)

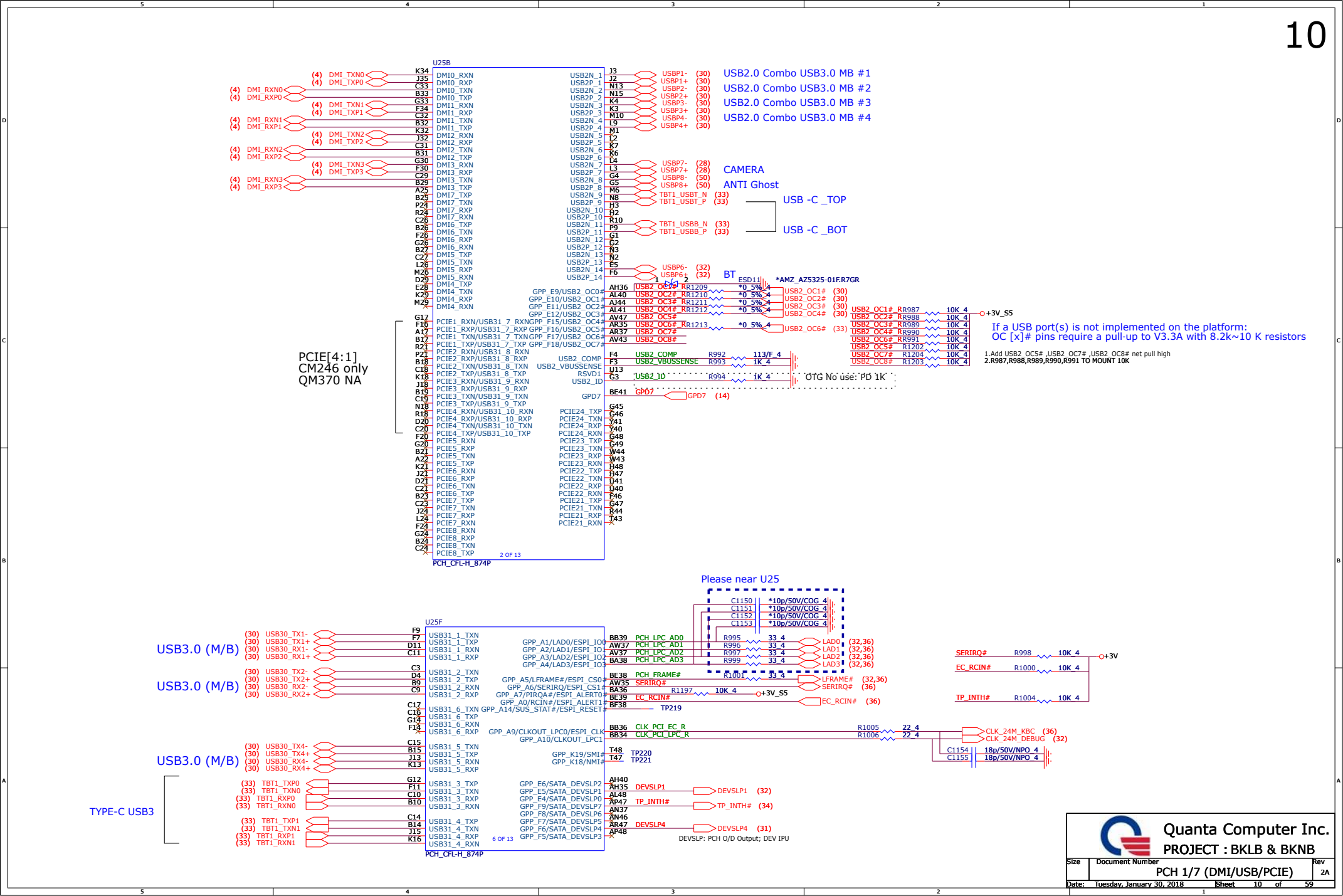


09

KBL-H Processor (RESERVED, CFG)



Quanta Computer Inc.			
PROJECT : BKLB & BKNB			
Size	Document Number		Rev
	CFL 7/7 (GND)		1A
Date: Tuesday, January 30, 2018	Sheet 959 of		



Quanta Computer Inc.		
PROJECT : BKLB & BKNB		
Size	Document Number	Rev
	PCH 1/7 (DMI/USB/PCIE)	2A
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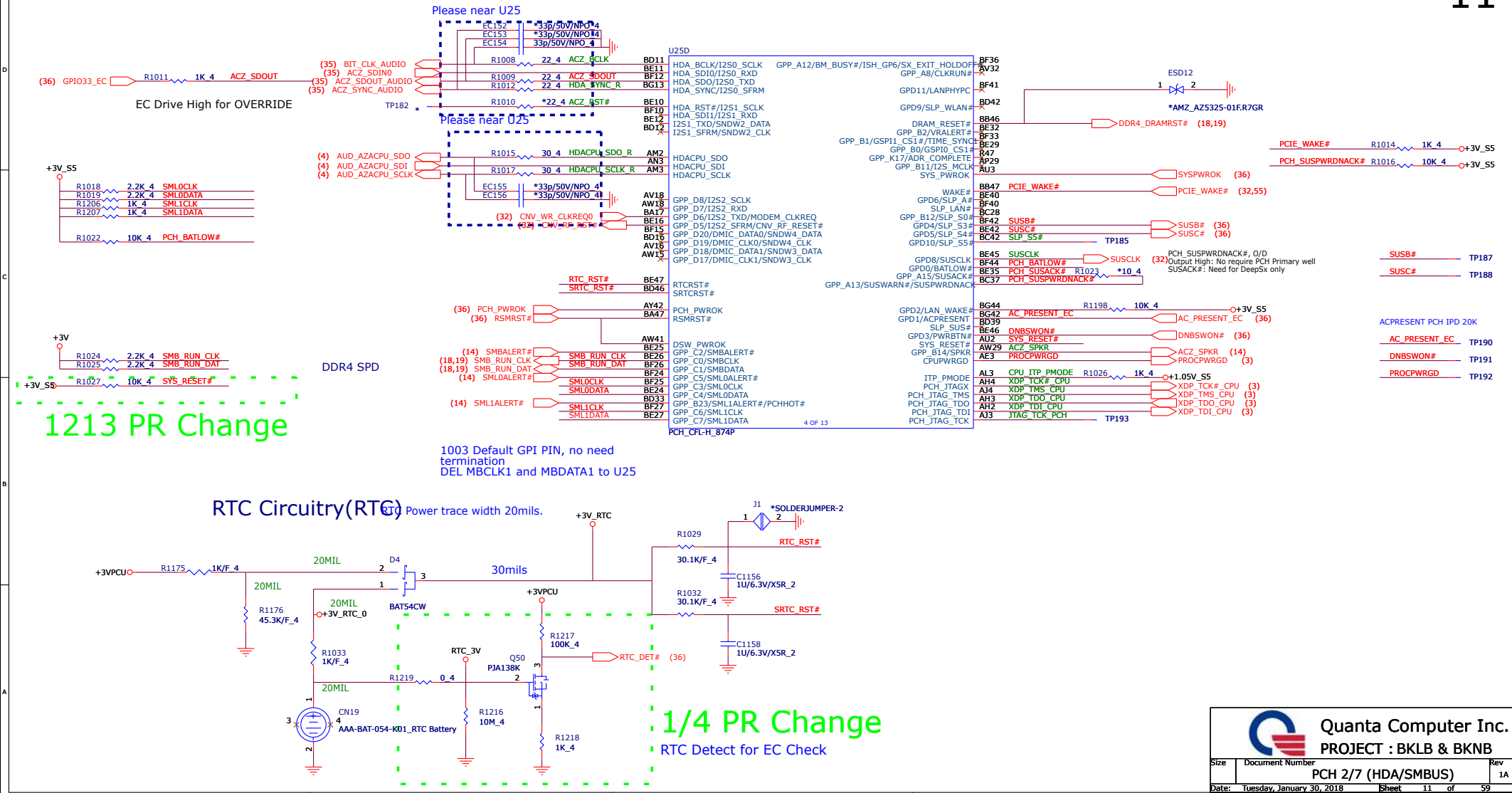

Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	PCH 2/7 (HDA/SMBUS)	1A
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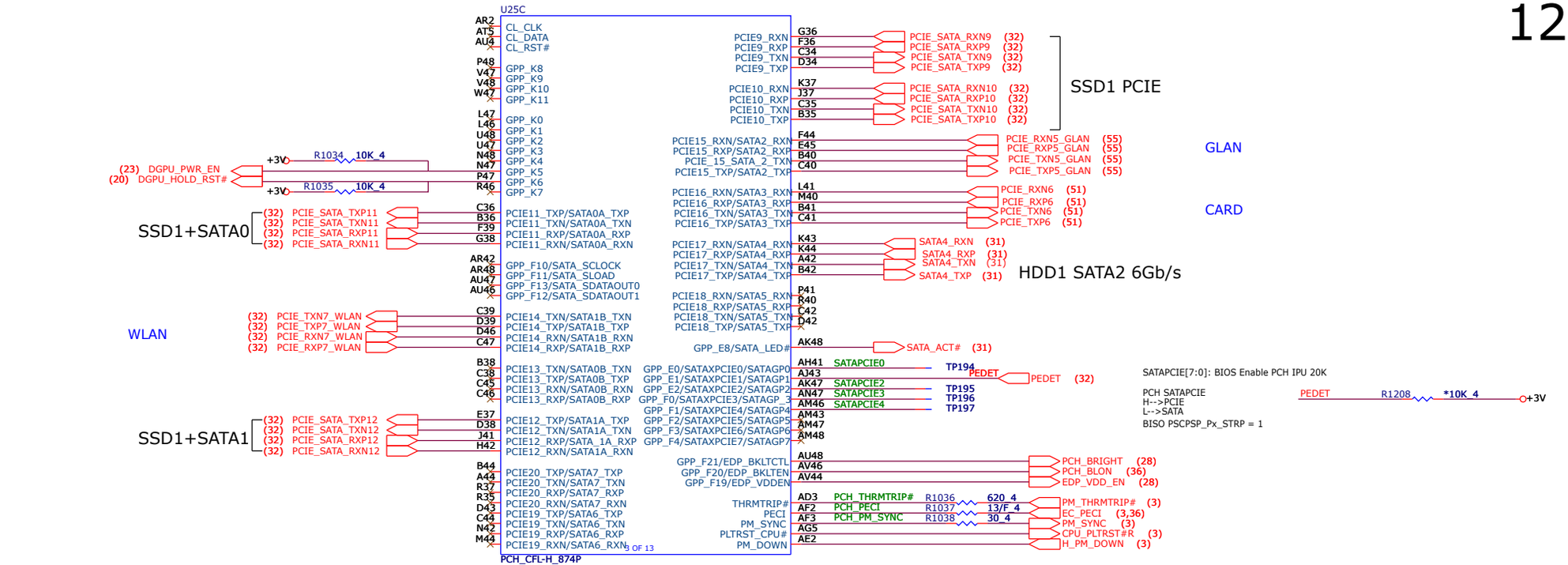

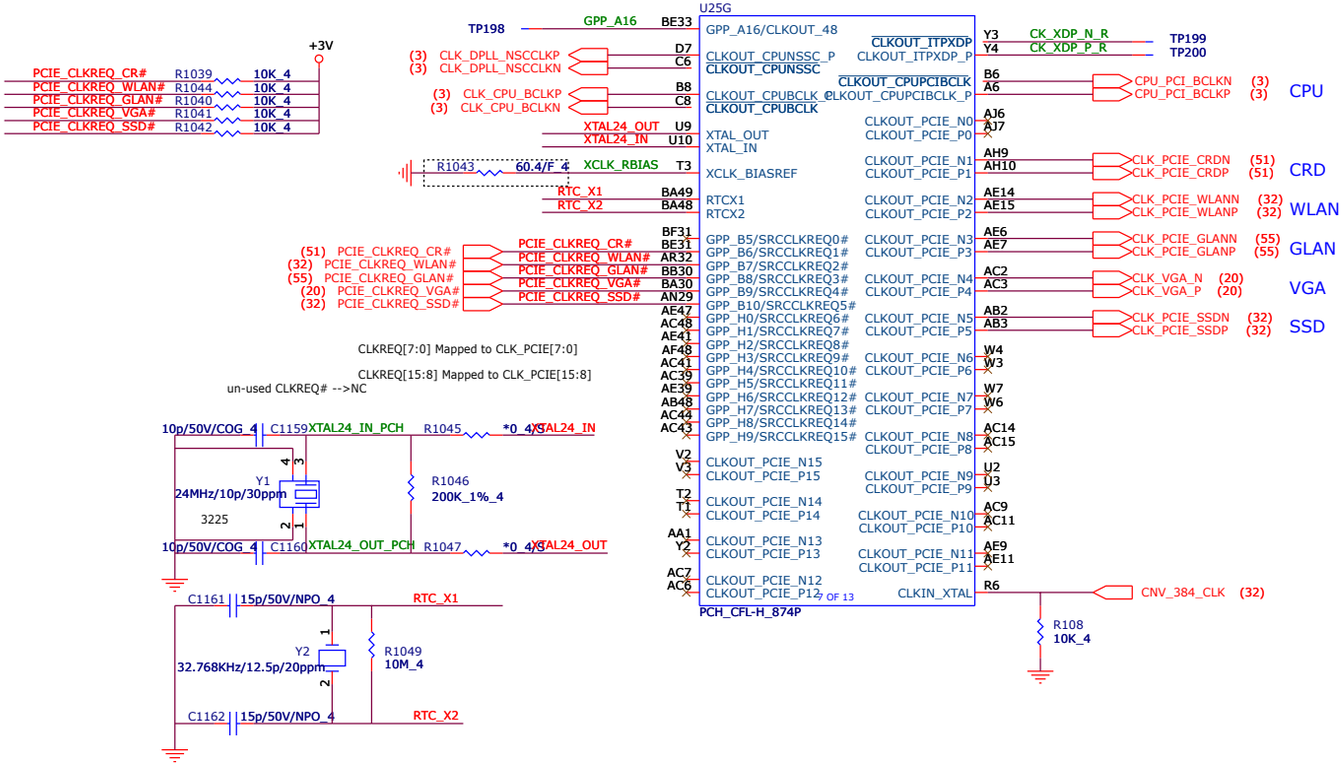

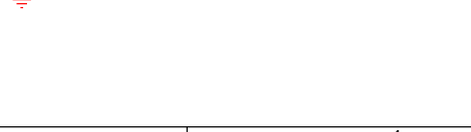

Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	PCH 3/7 (SATA/LPC/CLK)	1A
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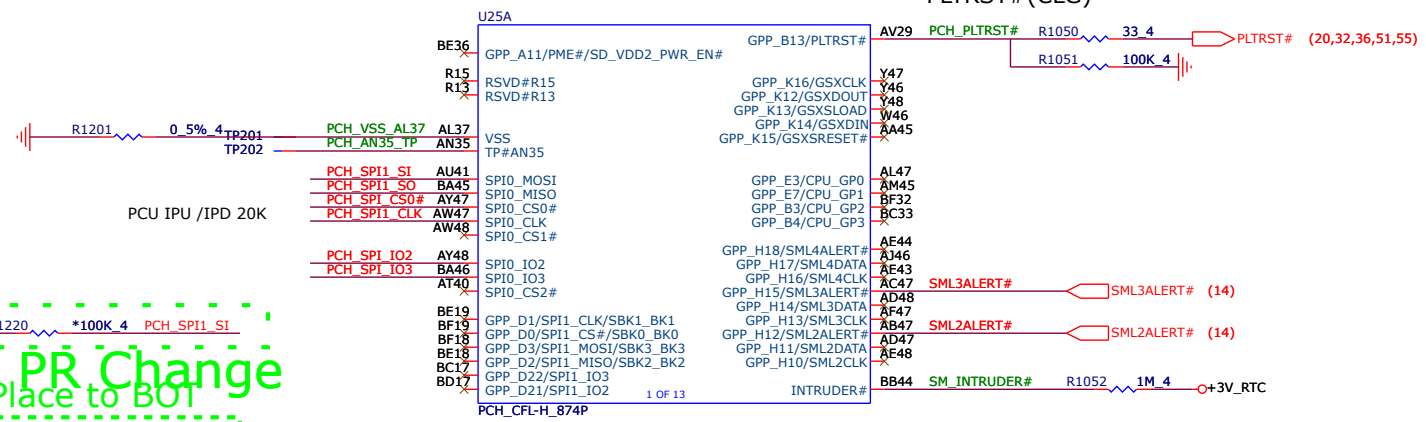
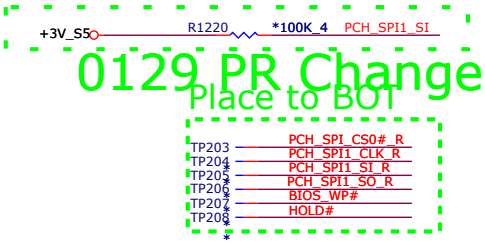
PLTRST#(CLG)

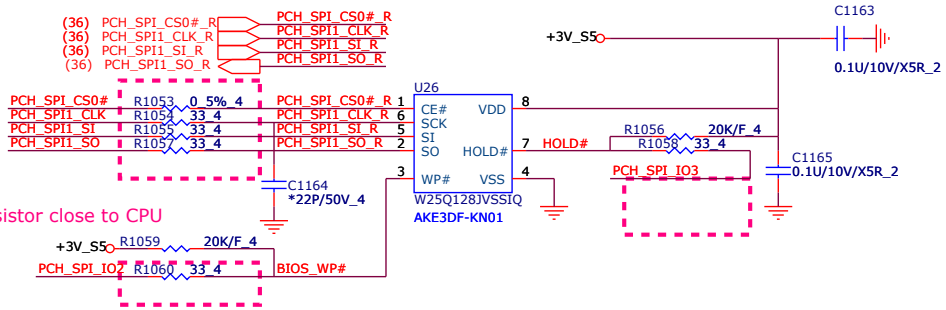


0129 PR Change

Place to BOT



PCH SPI ROM(CLG)



Put damping resistor close to CPU

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PROJECT : BKLB & BKNB

Size	Document Number	Rev
	PCH 4/7 (GPIO/MISC)	1A
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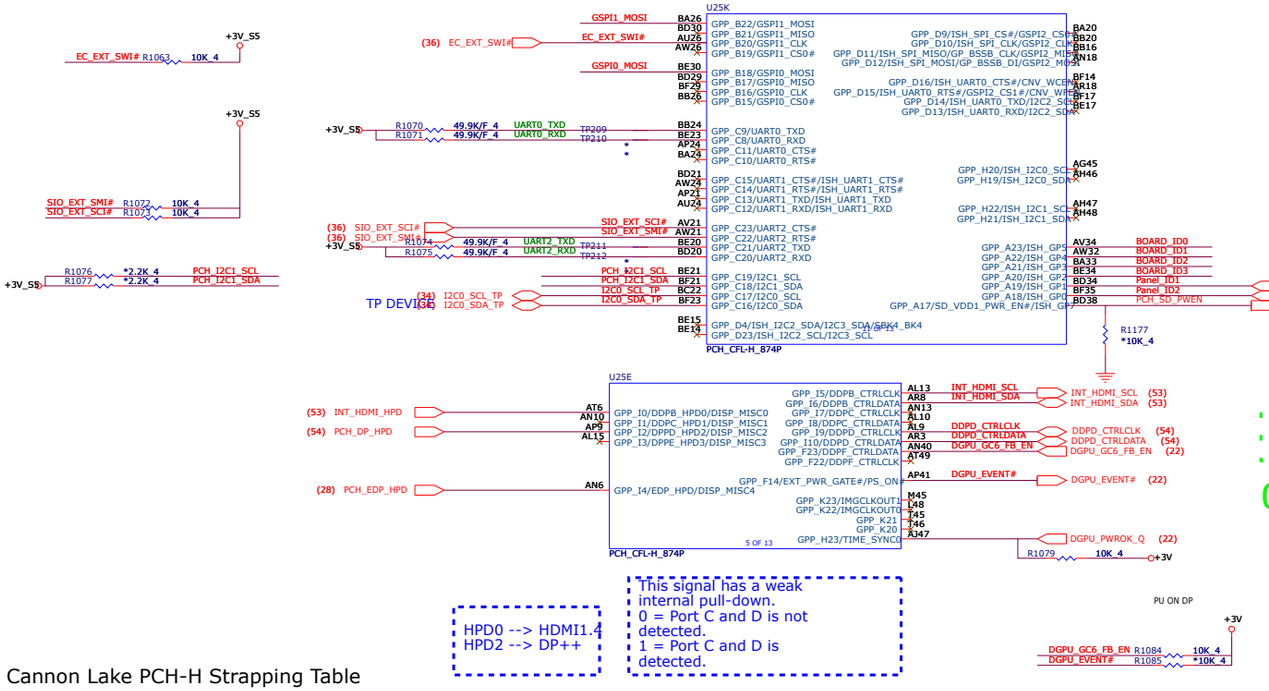


GPIO Pull-up/Pull-down(CLG)

R need place to BOT

R need place to BOT

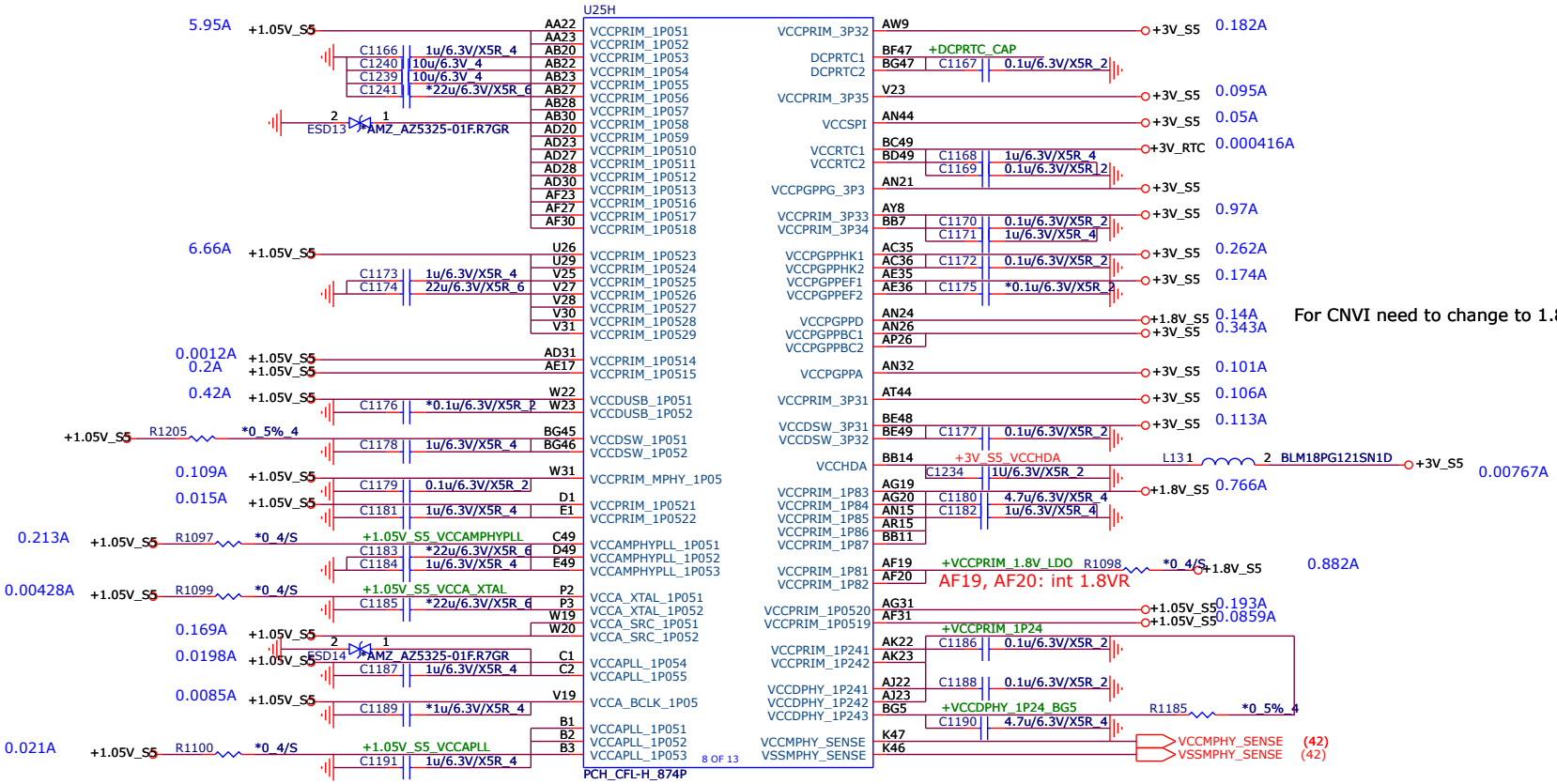
	Panel ID1	Panel ID2
FHD	11	
4K2K	1	0
HD	0	1

	BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3
GE15 1050TI ID1 ROG	00	0	0	
GE17 1050TI ID1 ROG	00	0	0	1
GD17 1050 ID1 ROG	0	0	10	
	0	0	11	
0104 PR Change	0	1	0	0
	0	1	0	1
	0	1	1	0
	0	1	1	1
	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	11	

Cannon Lake PCH-H Strapping Table

Pin Name	Strap description	Sampled	Configuration	xxx PCH STRAPS SETTING STATUS
GPP_B14 (SPKR)	Top Swap Override	PCH_PWROK	0 = *Disable Top Swap (iPD 20K) Default 1 = Enable Top Swap Mode	+3V_S5 R1086 *1K_4 ACZ_SPKR (11)
GPP_B18 (GSPI0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) Default 1 = Enable No Reboot Mode	+3V_S5 R1087 *1K_4 GSPI0_MOSI
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = *Disable Intel ME Cryp to TLS(iPD 20K) Default 1 = Enable Intel ME Cryp to TLS PU to support AMT TLS	+3V_S5 R1088 *1K_4 SMBALERT# (11)
GPP_B22 (GSPI1_MOSI)	Boot BIOS Strap Bit BBS	PCH_PWROK	0 = *SPI (iPD 20K) Default 1 = LPC	+3V_S5 R1089 *1K_4 GSPI1_MOSI
GPP_C5 (SML0ALERT#)	eSPI or LPC	RSMRST#	0 = *LPC is selected for EC (iPD 20K) Default 1 = eSPI selected for EC	TP213 SML0ALERT# (11)
SPI0_MOSI	Reserved	RSMRST#	(iPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
GPP_H15 (SML3ALERT#)	Reserved	RSMRST#	(iPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	TP214 SML3ALERT# (13)
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	(iPD 20K) This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.	TP215 SML1ALERT# (11)
SPI0_IO2	Reserved	RSMRST#	(iPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
SPI0_IO3	Reserved	RSMRST#	(iPU 15 ~ 40K) This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	
HDA_SDO (I2S0_TXD)	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = *Enable security in the Flash Description (iPD 20K) Default 1 = Disable Flash Descriptor Security (Override)	EC Drive High for OVERRIDE
GPP_H12 (SML2ALERT#)	eSPI Flash Sharing Mode	RSMRST#	0 = *Master Attached Flash Sharing (MAFS) enabled (iPD 20K)Default 1 = Slave Attached Flash Sharing (SAFS) enabled.	TP216 SML2ALERT# (13)
GPP_I6 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = *Port B is not detected (iPD 20K) (Default) 1 =Port B is detected	INT_HDMI_SCL R1090 2.2K_4 INT_HDMI_SDA R1091 2.2K_4 +3V
GPP_I8 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = *Port C is not detected (iPD 20K) (Default) 1 =Port C is detected	
GPP_I10 (DDPD_CTRLDATA)	Display Port D Detected	PCH_PWROK	0 = *Port D is not detected (iPD 20K) (Default) 1 =Port D is detected	DDPD_CTRLCLK R1094 2.2K_4 DDPD_CTRLDATA R1095 2.2K_4 +3V
GPP_F23	Display Port F Detected	PCH_PWROK	0 = *Port F is not detected (iPD 20K) (Default) 1 =Port F is detected	CFL - H CPU Not Support DDI Port F Change R1141 form 10K to 4.7K
GPP_J4 CNV_BRI_DT/ UART0_RTS#	XTAL Frequency Select	RSMRST#	An external pull-up is required on this strap since 38.4MHz XTAL is not supported on the PCH. 0 = *38.4MHz XTAL frequency selected. (iPD 20K) (Default) 1 = 24MHz XTAL frequency selected.	CNV_RBI_DT (16,32) +1.8V_S5 R1141 4.7K_4 R1142 *20K/F_4 PCH Strap: GPP_J4 = XTAL SELECT-1 HIGH -> 24 MHZ / LOW -> 38.4 MHZ
GPP_J6 CNV_RGI_DT/ UART0_TXD	M.2 CNV Mode Select	RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. (Default) 1 = Integrated CNVi disable.	CNV_RGI_DT (16,32) +1.8V_S5 R1143 20K/F_4 R1144 *20K/F_4 PCH Strap: GPP_J6 = M.2 CNVI STRAP HIGH -> DISABLE / LOW -> ENABLE
GPP_J9	1.8V VCCPSPI	RSMRST#	0 = *VCCSPI is connected to 3.3V rail. (iPD 20K) (Default) 1 = VCCSPI is connected to 1.8V rail	R1145 TP217 *10K_4 GPP_J9 (16) Note: If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os
GPD7	Reserved	DSW_PWROK	This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	External pull-up is required. Recommend 100K. +3V_S5 R1196 10K_4 GPD7 (10) R1146 *10K_4

Warning: This strap must be configured to '0' (SAFS is disabled) if the eSPI or LPC strap is configured to '0' (eSPI is disabled)



1.24V for CNVi logic = VCCDPHY_1P24 & +VCCPRIM_1P24
This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC.
Refer to the Platform Design Guide for implementation details.

Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	PCH 6/7 (POWER)	1A
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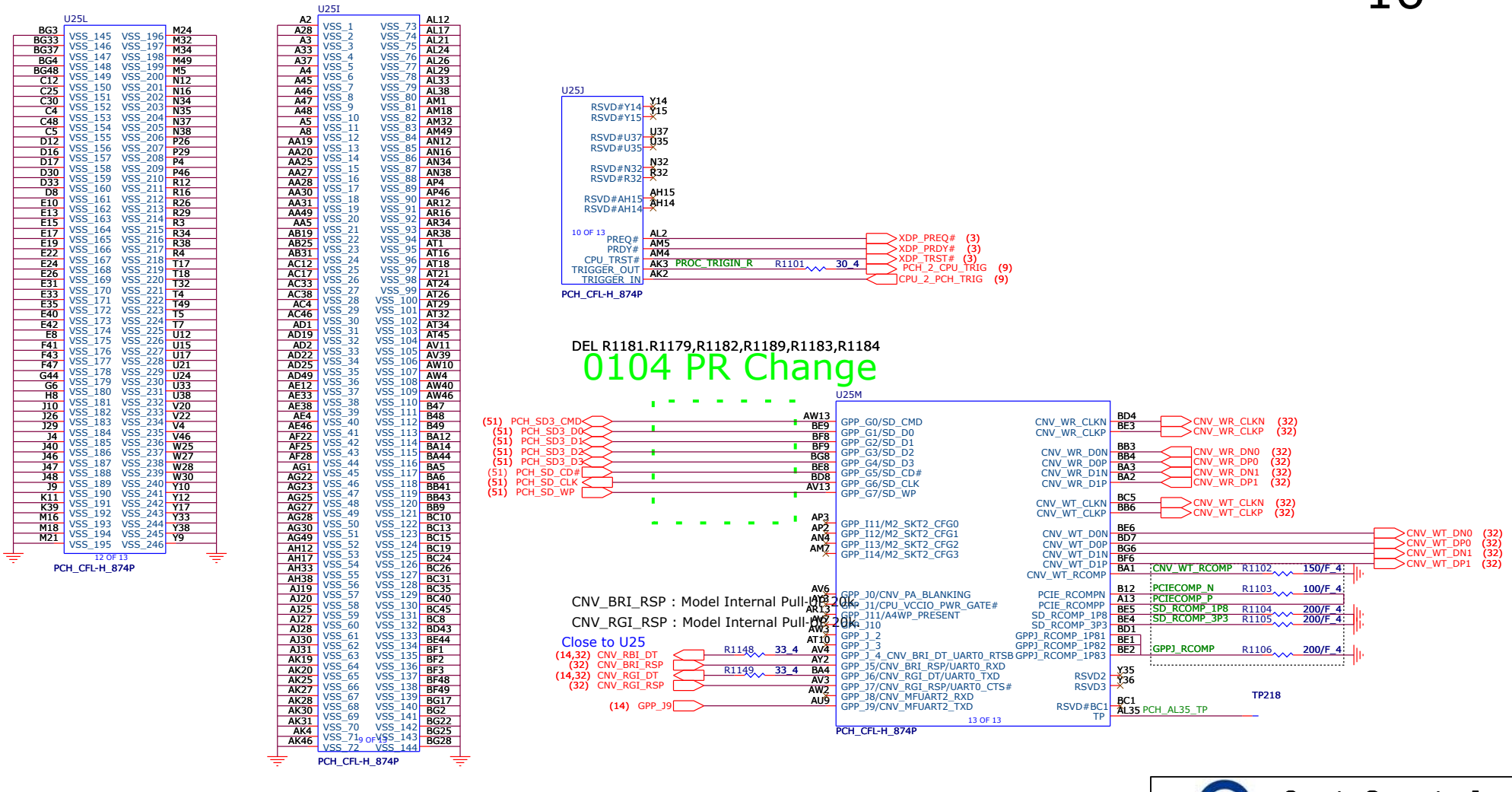

Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	PCH 7/7 (GND)	1A
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H2 *hole
H3 *hole
H4 *hole
H5 *hole
H34 *hole

SPAD1 *spad-re451x130np
SPAD2 *spad-bkna-1
SPAD3 *spad-bkna-2
SPAD4 *spad-bkna-3

placement on TOP SIDE VIN Plane

VIN
EMC3 6.8p/50V/NPO_4
C1077 0.1u/25V_2
C1078 0.1u/25V_2
C1079 0.1u/25V_2
C1080 0.1u/25V_2
C1081 0.1u/25V_2
C1082 0.1u/25V_2
C1085 0.1u/25V_2
C1086 0.1u/25V_2
EMC9 0.1u/25V_2

H12 *hole
H17 *hole
H24 *hole
H35 *hole
EMIR1 *0_6S
LANGND

0129 PR Change

For EMI place TOP

+3V C1144 *0.1u/25V_2

Reserve for EMI

H38 *HOLE
H39 *HOLE
H40 *HOLE
H42 *SPAD-BKNB-1
H1 *hole

EMI1 HOLE
EMI2 *HOLE
EMI3 *HOLE
EMI4 *HOLE

For EMI add Gasket

+3VPCU EMC10 0.1u/25V_4 For EMI place BOT
+3V_RTC EMC11 0.1u/25V_4 For EMI place BOT

SPAD8 *SPAD-RE112X289

+1.2V_SUS
C1242 *0.1u/6.3V/X5R_2
C1243 *0.1u/6.3V/X5R_2
C1244 *0.1u/6.3V/X5R_2
C1245 *0.1u/6.3V/X5R_2
C1246 0.01U/50V_4
C1247 0.01U/50V_4
C1248 0.01U/50V_4
C1249 0.01U/50V_4

placement on TOP SIDE VA+ Plane

VA+
C1083 0.1U/50V/X5R_4
C1084 0.1U/50V/X5R_4
EMC4 6.8p/50V/NPO_4

H45 *HOLE
H54 *HOLE

H36 HOLE WLAN NUT
H9 HOLE SSD NUT

+3V_S5
C1108 1000p/50V_4
C1107 1000p/50V_4
C1110 1000p/50V_4
C1109 1000p/50V_4

+3V_S5 +5V
C1103 1000p/50V_4
C1104 1000p/50V_4
C1106 1000p/50V_4
C1105 1000p/50V_4

+5V +5V_S5
C1112 1000p/50V_4
C1111 1000p/50V_4
C1114 1000p/50V_4
C1113 1000p/50V_4

H13 *hole
EMCJG34 *1u/25V_6

H33 *HOLE
H55 *HOLE
H44 *hole
H43 *HOLE
EMCJG33 *1u/25V_6
EMCJG32 *1u/25V_6
EMCJG30 *1u/25V_6
EMCJG31 *1u/25V_6

+3V_S5
C1133 1000p/50V_4
C1131 1000p/50V_4
C1134 1000p/50V_4
C1132 1000p/50V_4

+3V_S5 +5V
C1128 1000p/50V_4
C1127 1000p/50V_4
C1130 1000p/50V_4
C1129 1000p/50V_4

+5V +5V_S5
C1124 1000p/50V_4
C1123 1000p/50V_4
C1126 1000p/50V_4
C1125 1000p/50V_4

For ESD request

H46 *hole
EMCJG2 EMCJG3 EMCJG4 EMCJG12 EMCJG10 EMCJG11
EMCJG21 *1u/25V_6
EMCJG9 *0_6S
*SHORT_ PAD9212 *short92x32 *SHORT_ PAD9212 *short92x32 *SHORT_ PAD9212 *short92x32

H47 *HOLE
H48 *HOLE
H49 *HOLE
EMCJG29 1u/25V_6
EMCJG28 1u/25V_6
EMCJG27 1u/25V_6

H15 *hole
BOT side
TOP side
EMCJG22 1u/25V_6
EMCJG23 1u/25V_6

+5V_S5
C1135 1000p/50V_4
C1136 1000p/50V_4
C1138 1000p/50V_4
C1137 1000p/50V_4

+5V_S5
C1119 1000p/50V_4
C1120 1000p/50V_4
C1122 1000p/50V_4
C1121 1000p/50V_4

H53 *hole
EMCJG6 EMCJG8 EMCJG7 EMCJG16 EMCJG15 EMCJG14 EMCJG13
*short92x32 *0_6S *0_6S *0_6S *1u/25V_6 *1u/25V_6 *1u/25V_6

H50 *HOLE
H51 *HOLE
H52 *HOLE
EMCJG26 1u/25V_6
EMCJG25 1u/25V_6
EMCJG24 1u/25V_6

H37 HOLE Ship mode NUT
EMCJG19 EMCJG20 EMCJG17 EMCJG18 *1u/25V_6
*SHORT_ PAD9212 *SHORT_ PAD9212 *SHORT_ PAD9212

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	HOLE	1A
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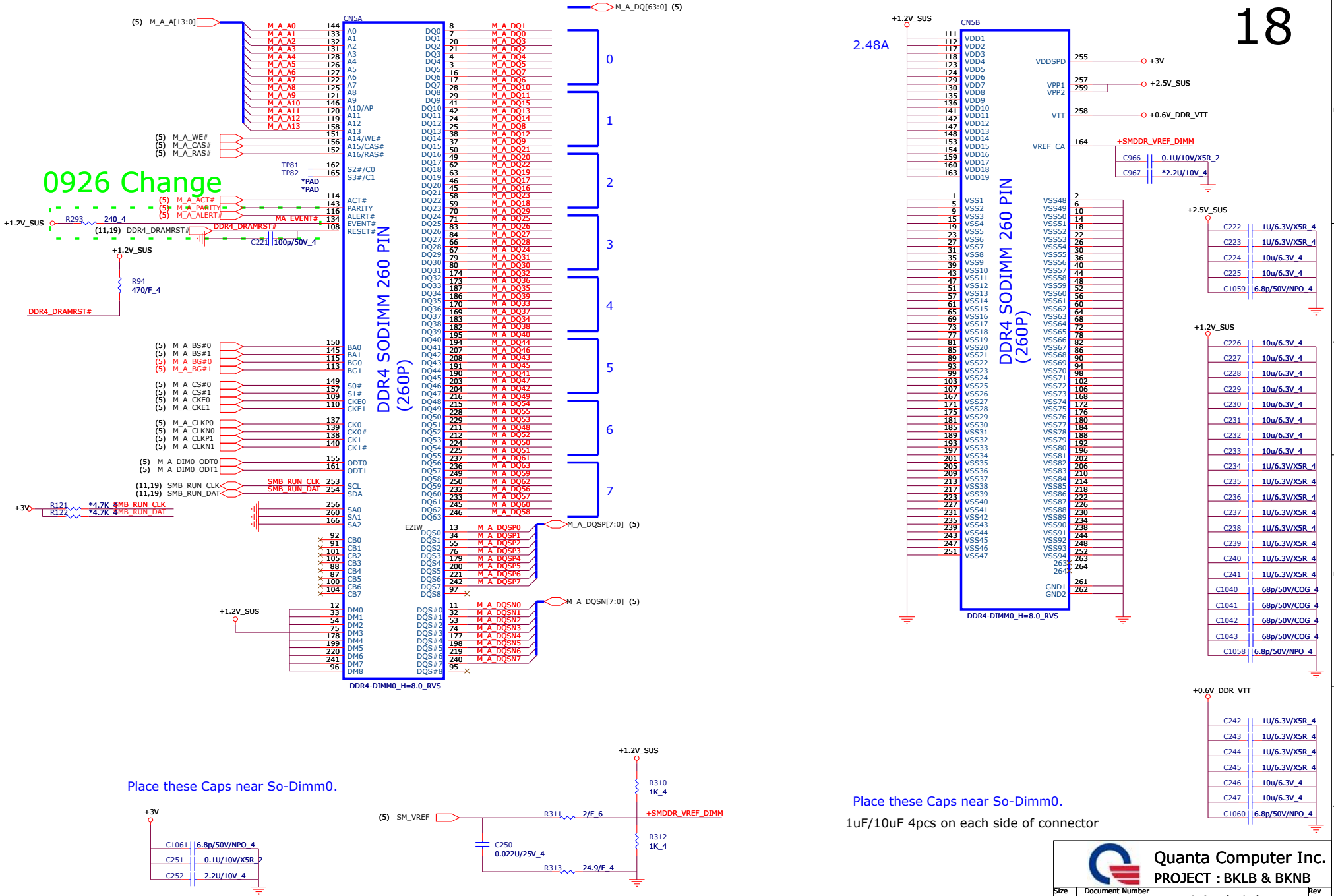

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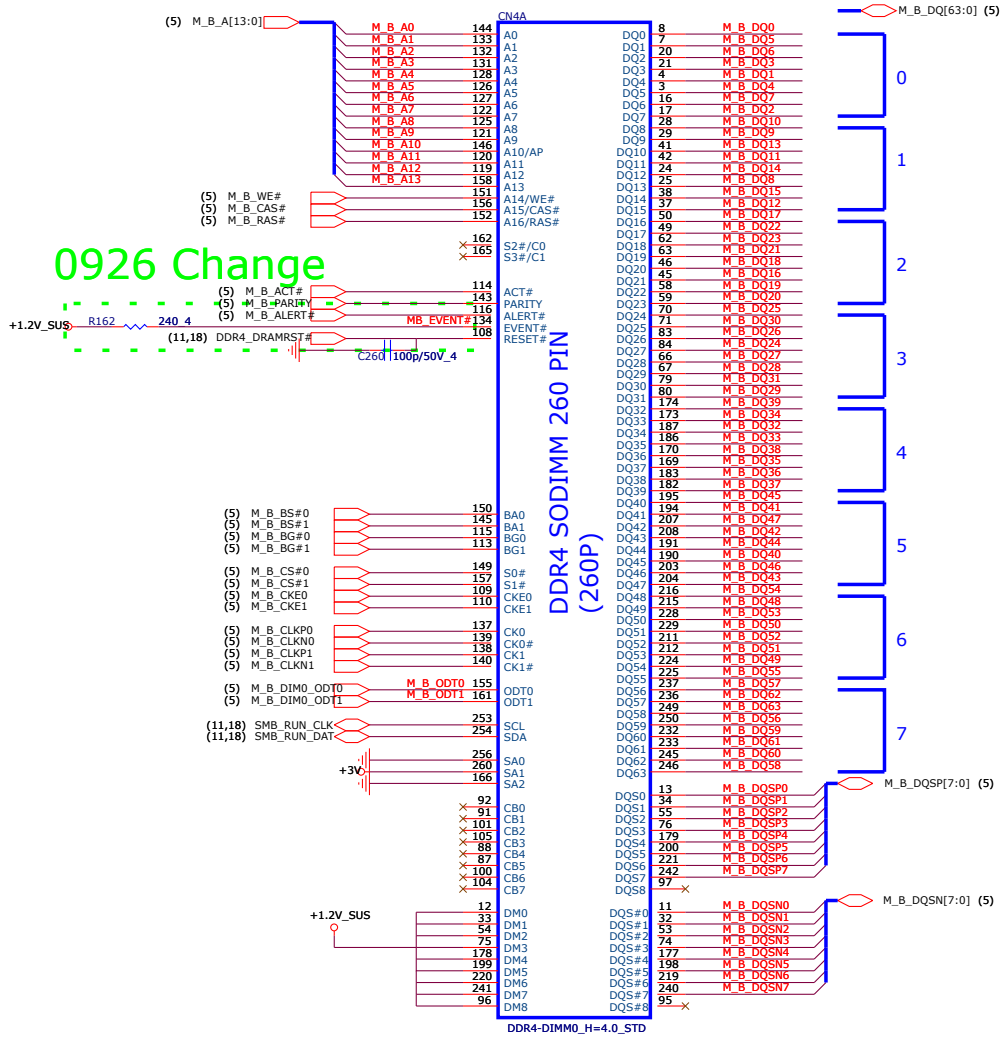
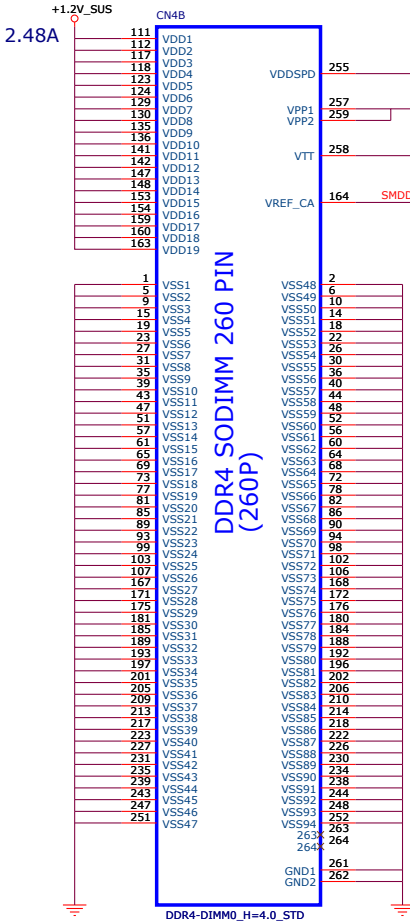
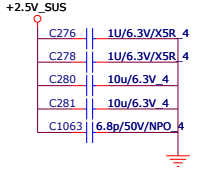
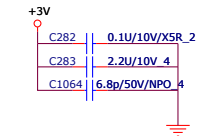
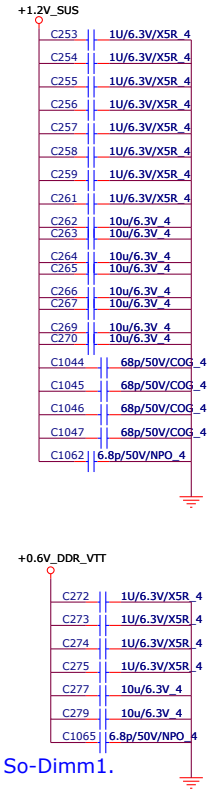






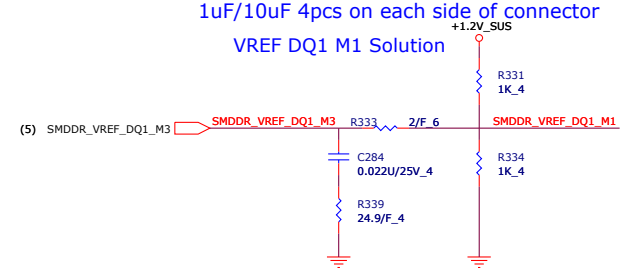




Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector

VREF DQ1 M1 Solution



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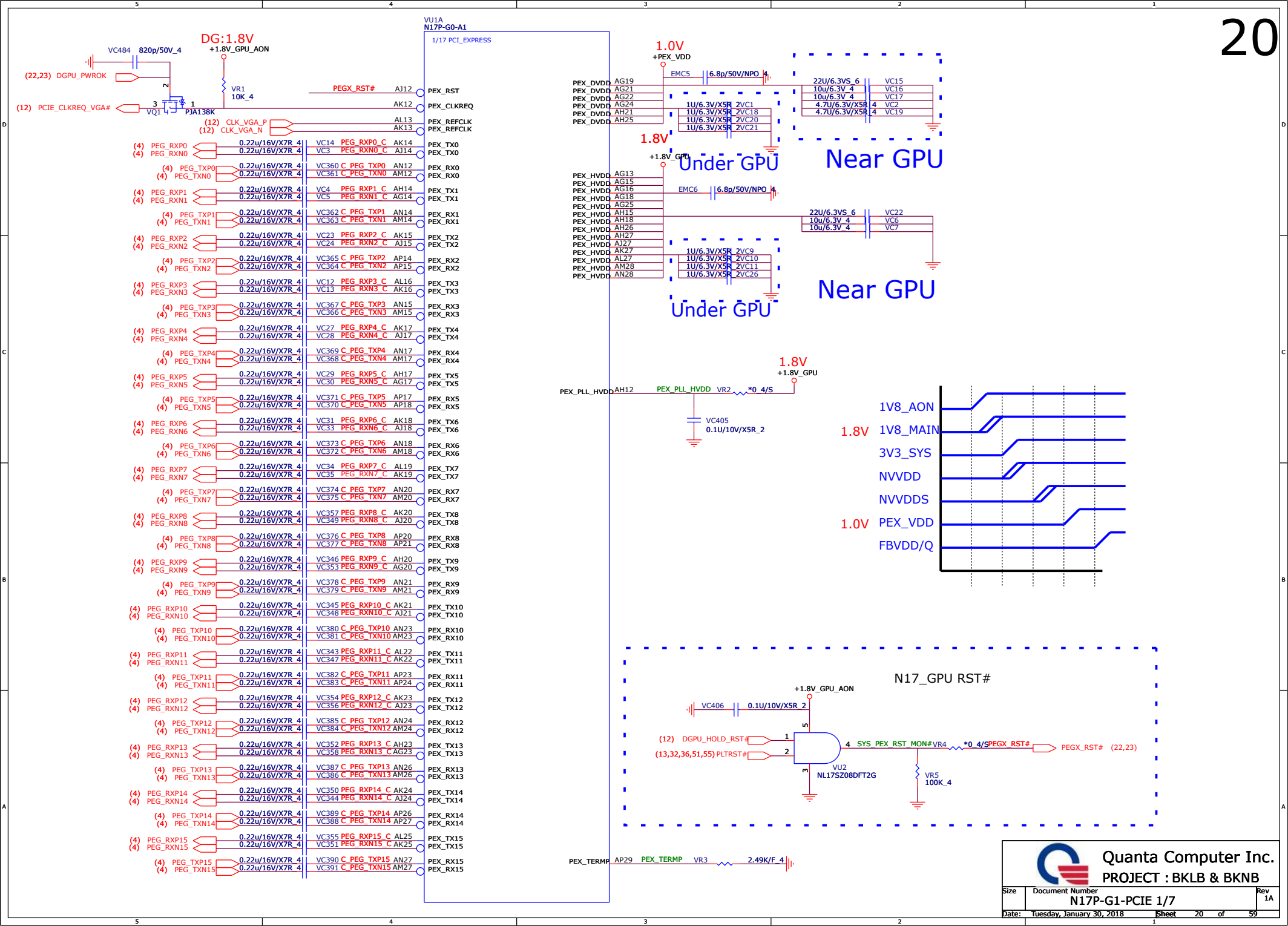

(4) PEG_RXP0 / (4) PEG_RXN0	0.22u/16V/X7R_4	VC14 PEG_RXP0_C AK14 / VC3 PEG_RXN0_C AJ14	PEX_TX0 / PEX_TX0
(4) PEG_TXP0 / (4) PEG_TXN0	0.22u/16V/X7R_4	VC360 C_PEG_TXP0 AN12 / VC361 C_PEG_TXN0 AM12	PEX_RX0 / PEX_RX0
(4) PEG_RXP1 / (4) PEG_RXN1	0.22u/16V/X7R_4	VC4 PEG_RXP1_C AH14 / VC5 PEG_RXN1_C AG14	PEX_TX1 / PEX_TX1
(4) PEG_TXP1 / (4) PEG_TXN1	0.22u/16V/X7R_4	VC362 C_PEG_TXP1 AN14 / VC363 C_PEG_TXN1 AM14	PEX_RX1 / PEX_RX1
(4) PEG_RXP2 / (4) PEG_RXN2	0.22u/16V/X7R_4	VC23 PEG_RXP2_C AK15 / VC24 PEG_RXN2_C AJ15	PEX_TX2 / PEX_TX2
(4) PEG_TXP2 / (4) PEG_TXN2	0.22u/16V/X7R_4	VC365 C_PEG_TXP2 AP14 / VC364 C_PEG_TXN2 AP15	PEX_RX2 / PEX_RX2
(4) PEG_RXP3 / (4) PEG_RXN3	0.22u/16V/X7R_4	VC12 PEG_RXP3_C AL16 / VC13 PEG_RXN3_C AK16	PEX_TX3 / PEX_TX3
(4) PEG_TXP3 / (4) PEG_TXN3	0.22u/16V/X7R_4	VC367 C_PEG_TXP3 AN15 / VC366 C_PEG_TXN3 AM15	PEX_RX3 / PEX_RX3
(4) PEG_RXP4 / (4) PEG_RXN4	0.22u/16V/X7R_4	VC27 PEG_RXP4_C AK17 / VC28 PEG_RXN4_C AJ17	PEX_TX4 / PEX_TX4
(4) PEG_TXP4 / (4) PEG_TXN4	0.22u/16V/X7R_4	VC369 C_PEG_TXP4 AN17 / VC368 C_PEG_TXN4 AM17	PEX_RX4 / PEX_RX4
(4) PEG_RXP5 / (4) PEG_RXN5	0.22u/16V/X7R_4	VC29 PEG_RXP5_C AH17 / VC30 PEG_RXN5_C AG17	PEX_TX5 / PEX_TX5
(4) PEG_TXP5 / (4) PEG_TXN5	0.22u/16V/X7R_4	VC371 C_PEG_TXP5 AP17 / VC370 C_PEG_TXN5 AP18	PEX_RX5 / PEX_RX5
(4) PEG_RXP6 / (4) PEG_RXN6	0.22u/16V/X7R_4	VC31 PEG_RXP6_C AK18 / VC33 PEG_RXN6_C AJ18	PEX_TX6 / PEX_TX6
(4) PEG_TXP6 / (4) PEG_TXN6	0.22u/16V/X7R_4	VC373 C_PEG_TXP6 AN18 / VC372 C_PEG_TXN6 AM18	PEX_RX6 / PEX_RX6
(4) PEG_RXP7 / (4) PEG_RXN7	0.22u/16V/X7R_4	VC34 PEG_RXP7_C AL19 / VC35 PEG_RXN7_C AK19	PEX_TX7 / PEX_TX7
(4) PEG_TXP7 / (4) PEG_TXN7	0.22u/16V/X7R_4	VC374 C_PEG_TXP7 AN20 / VC375 C_PEG_TXN7 AM20	PEX_RX7 / PEX_RX7
(4) PEG_RXP8 / (4) PEG_RXN8	0.22u/16V/X7R_4	VC357 PEG_RXP8_C AK20 / VC349 PEG_RXN8_C AJ20	PEX_TX8 / PEX_TX8
(4) PEG_TXP8 / (4) PEG_TXN8	0.22u/16V/X7R_4	VC376 C_PEG_TXP8 AP20 / VC377 C_PEG_TXN8 AP21	PEX_RX8 / PEX_RX8
(4) PEG_RXP9 / (4) PEG_RXN9	0.22u/16V/X7R_4	VC346 PEG_RXP9_C AH20 / VC353 PEG_RXN9_C AG20	PEX_TX9 / PEX_TX9
(4) PEG_TXP9 / (4) PEG_TXN9	0.22u/16V/X7R_4	VC378 C_PEG_TXP9 AN21 / VC379 C_PEG_TXN9 AM21	PEX_RX9 / PEX_RX9
(4) PEG_RXP10 / (4) PEG_RXN10	0.22u/16V/X7R_4	VC345 PEG_RXP10_C AK21 / VC348 PEG_RXN10_C AJ21	PEX_TX10 / PEX_TX10
(4) PEG_TXP10 / (4) PEG_TXN10	0.22u/16V/X7R_4	VC380 C_PEG_TXP10 AN23 / VC381 C_PEG_TXN10 AM23	PEX_RX10 / PEX_RX10
(4) PEG_RXP11 / (4) PEG_RXN11	0.22u/16V/X7R_4	VC343 PEG_RXP11_C AL22 / VC347 PEG_RXN11_C AK22	PEX_TX11 / PEX_TX11
(4) PEG_TXP11 / (4) PEG_TXN11	0.22u/16V/X7R_4	VC382 C_PEG_TXP11 AP23 / VC383 C_PEG_TXN11 AP24	PEX_RX11 / PEX_RX11
(4) PEG_RXP12 / (4) PEG_RXN12	0.22u/16V/X7R_4	VC354 PEG_RXP12_C AK23 / VC356 PEG_RXN12_C AJ23	PEX_TX12 / PEX_TX12
(4) PEG_TXP12 / (4) PEG_TXN12	0.22u/16V/X7R_4	VC385 C_PEG_TXP12 AN24 / VC384 C_PEG_TXN12 AM24	PEX_RX12 / PEX_RX12
(4) PEG_RXP13 / (4) PEG_RXN13	0.22u/16V/X7R_4	VC352 PEG_RXP13_C AH23 / VC358 PEG_RXN13_C AG23	PEX_TX13 / PEX_TX13
(4) PEG_TXP13 / (4) PEG_TXN13	0.22u/16V/X7R_4	VC387 C_PEG_TXP13 AN26 / VC386 C_PEG_TXN13 AM26	PEX_RX13 / PEX_RX13
(4) PEG_RXP14 / (4) PEG_RXN14	0.22u/16V/X7R_4	VC350 PEG_RXP14_C AK24 / VC344 PEG_RXN14_C AJ24	PEX_TX14 / PEX_TX14
(4) PEG_TXP14 / (4) PEG_TXN14	0.22u/16V/X7R_4	VC389 C_PEG_TXP14 AP26 / VC388 C_PEG_TXN14 AP27	PEX_RX14 / PEX_RX14
(4) PEG_RXP15 / (4) PEG_RXN15	0.22u/16V/X7R_4	VC355 PEG_RXP15_C AL25 / VC351 PEG_RXN15_C AK25	PEX_TX15 / PEX_TX15
(4) PEG_TXP15 / (4) PEG_TXN15	0.22u/16V/X7R_4	VC390 C_PEG_TXP15 AN27 / VC391 C_PEG_TXN15 AM27	PEX_RX15 / PEX_RX15

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	N17P-G1-PCIE 1/7	1A
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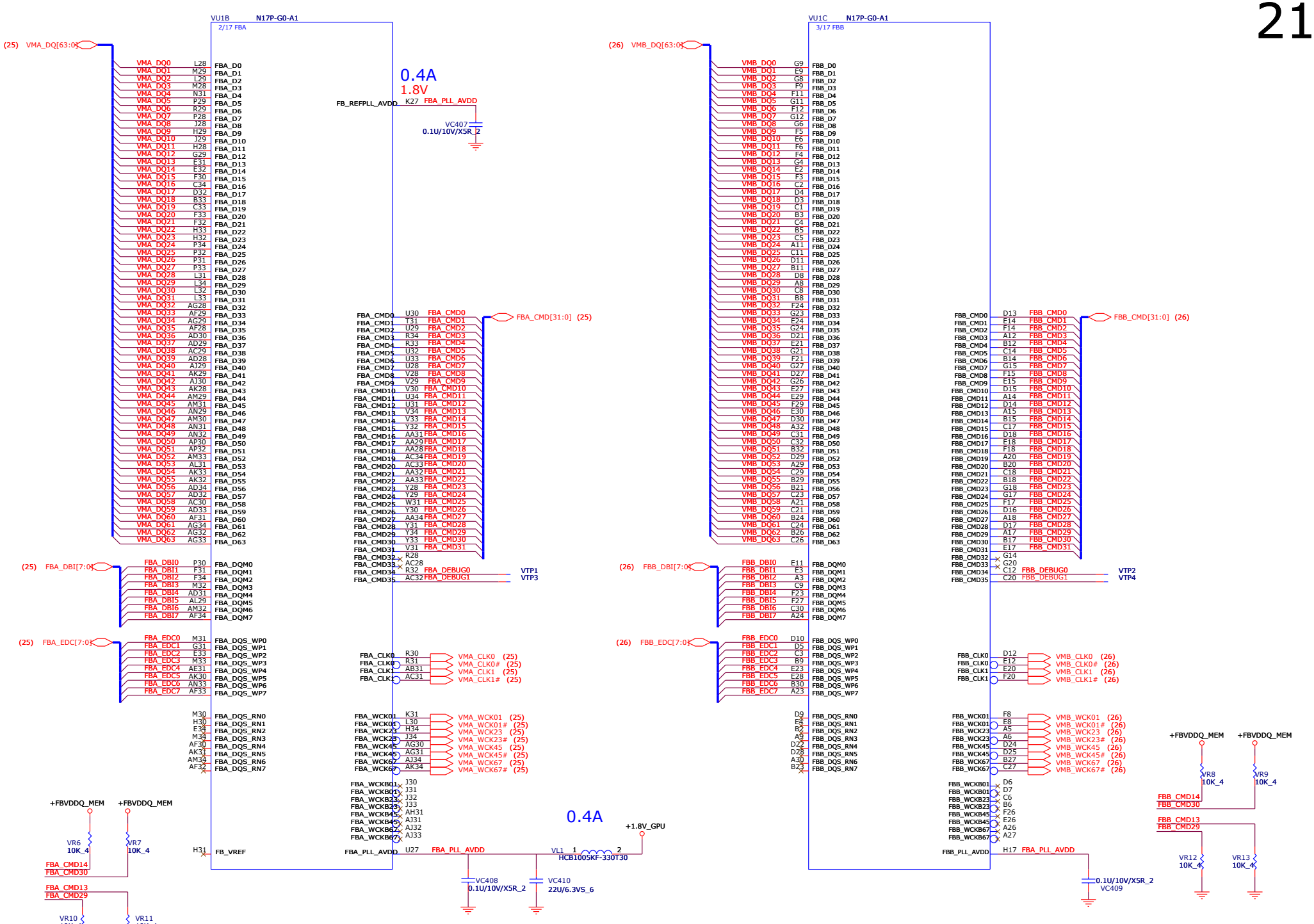

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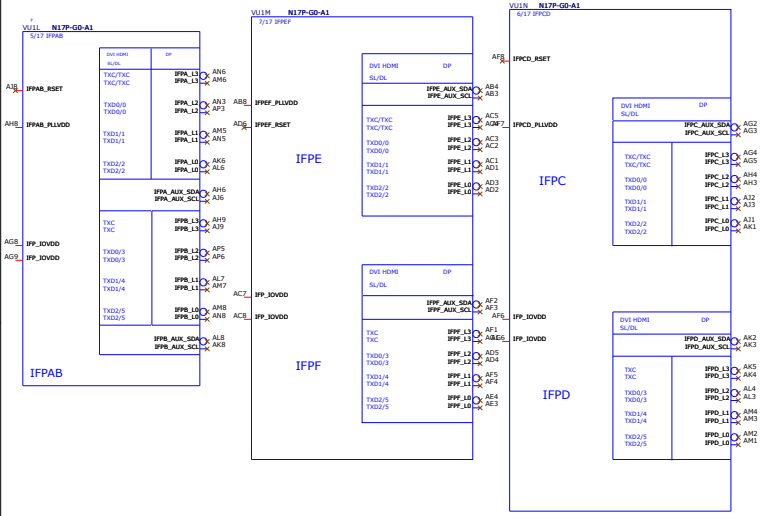
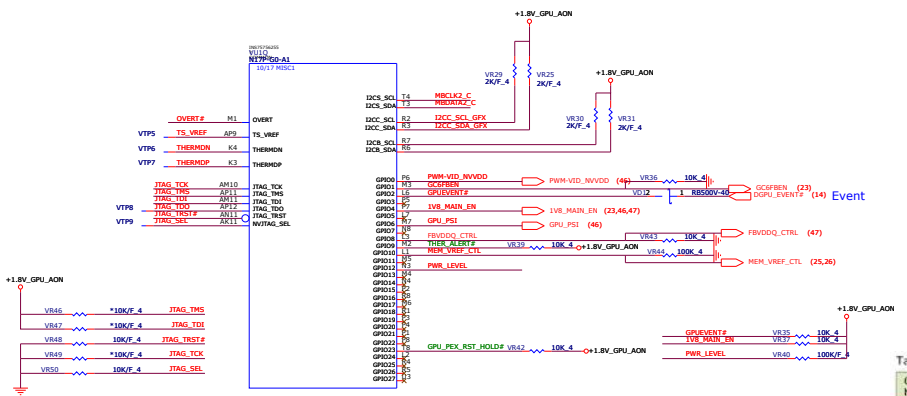
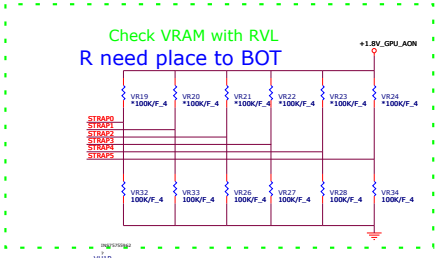




STRAP[2:0] VRAM Table for N17P-G0/G1 GDDR5 Recommended Memories

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	Quanta P/N	FBVDD/Q	
0x0	GDDR5 256Mx32 7 GHz	Samsung	SAMSUNG/K4G80325FB-HC28	AKG5QGDT515	1.5V	Default
0x1	GDDR5 256Mx32 7 GHz	Micron MICRON/MT51J256M32HF-70:A		AKG5QGUTL10	1.5V	
0x7	GDDR5 128Mx32 7 GHz	Samsung	SAMSUNG/K4G41325FE-HC28	AKG5PGUT508	1.5V	
0x8	GDDR5 128Mx32 7 GHz	ELPIDA ELPIDA/EDW4032BABG-70-F-D		AKG5PW0TL12	1.55V	



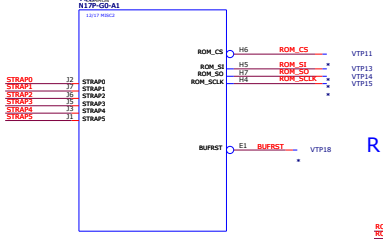
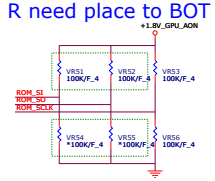


Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)



GFx SMBus Isolation(for EC)

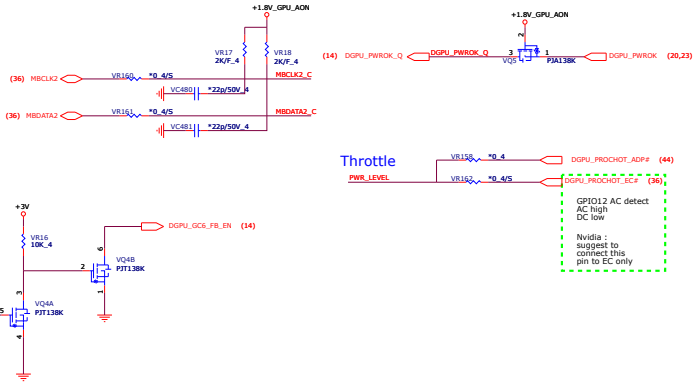


Table 14.2 GPIO Descriptions for GB4C-128 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	0 to1V8 PWM output
GPIO1	GC6M: GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source 10 KΩ pull-down
GPIO2	GC6M: GPU_EVENT#/ WAKE*	I	GPU wake signal for GC6 2.1	10KΩ pull-up to 1V8_AON, unless driven actively.
GPIO3	NVVDD_SRAM_PWM	O	PWM output to control the SRAM power supply	0 to 1V8 output
GPIO4	GC6M:1V8_MAIN_EN	O	GPU power sequencing for GC6 2.1	Open Drain 10KΩ pull-up to 1V8_AON
GPIO5	FRM_LCK	I	Active low Frame Lock	Open Drain 1V8 pull-up to 1V8AON

Table 14.2 GPIO Descriptions for GB4C-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO6	NVVDD_PSI	O	Phase Shedding (see Section 14.3.3)	10 kΩ pull-up to 1V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VDD Quadro:Power_Brake#	O	Panel Power enable	100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 kΩ pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	LCD Panel Backlight Enable	Panel Backlight Enable
GPIO14	HPD_IFPA	I	Hot Plug Detect for IFPA	Inverted Input. See Figure 14.5
GPIO15	HPD_IFPB	I	Hot Plug Detect for IFPB	Inverted Input. See Figure 14.5
GPIO16	GC6M: GPU_PEX_RST_HOLD#	O	System side PCIe reset monitor	10 kΩ pull-up to 1V8_AON unless actively driven
GPIO17	HPD_IFPD	I	Hot Plug Detect for IFPD	Inverted Input. See Figure 14.5
GPIO18	HPD_IFPE	I	Hot Plug Detect for IFPE	Inverted Input. See Figure 14.5
GPIO19	3D Vision	O	3D Vision L/R Signal	100 kΩ pull-down
GPIO20	PCES_MODE			
GPIO21	UNUSED	I/O		
GPIO22	UNUSED	I/O		

Table 14.2 GPIO Descriptions for GB4C-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO23	GC6M: GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	Open Drain 10 kΩ pull-up to a gated 3V3
GPIO24	HPD_IFPF	I	Hot plug detect for IFPF	Inverted input. See Figure 14.5
GPIO25	UNUSED			
GPIO26	UNUSED			
GPIO27	HPD_IFPC	I	Hot plug detect for IFPC	Inverted input. See Figure 14.5

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON

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Under GPU

Near GPU

NVVDD POWER GOOD LOOPBACK

DEL NVVDDSPG

0110 PR Change

Change VR67 from 100K to 150K

Overt temp ckt for NVVDD

for GC6

GPU All power good

0.4A

90 ohms +/- 15% Differential Impedance

For Power off sequence

0110 PR Change

Add power off timing

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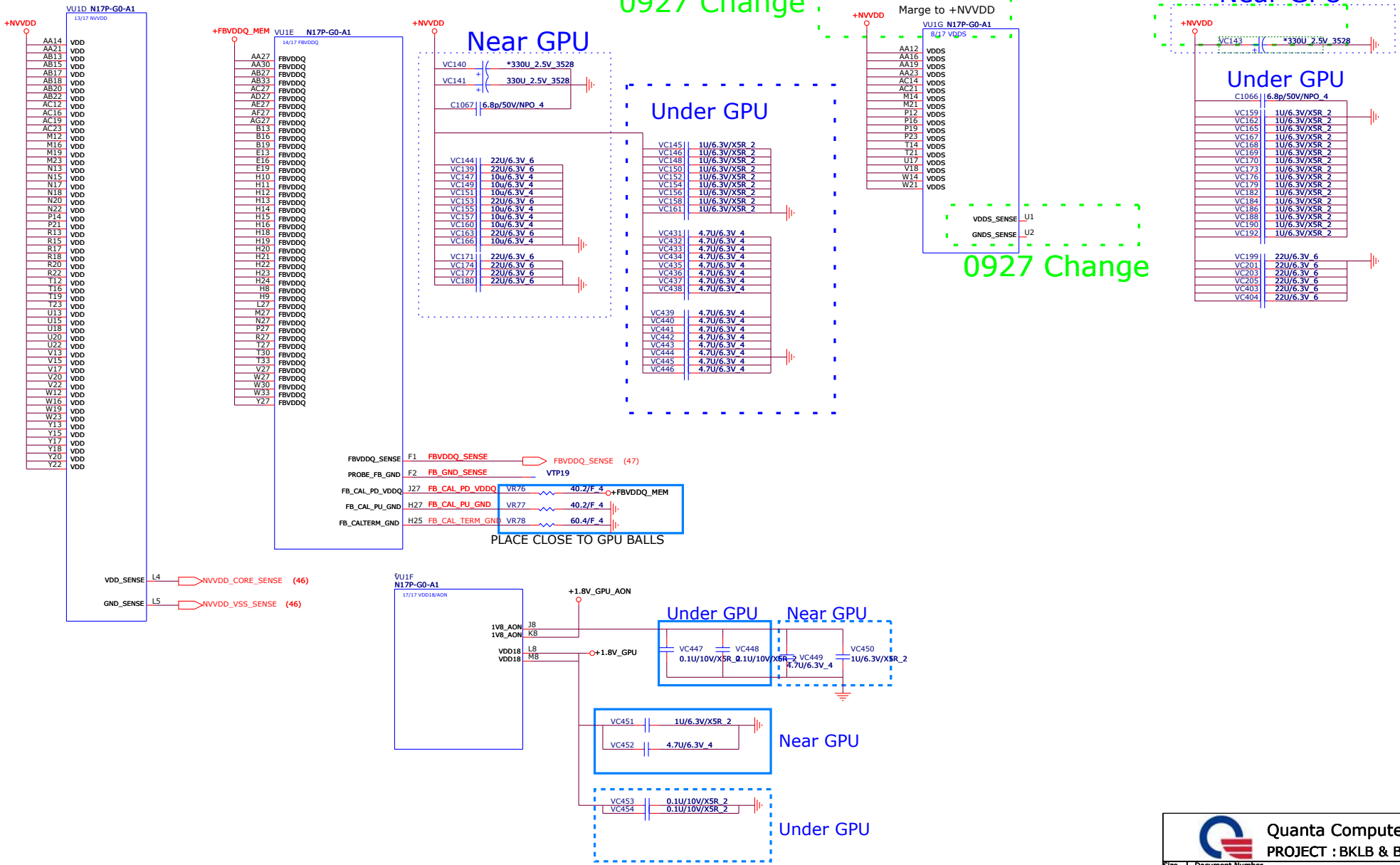
0927 Change
Marge to +NVVDD
Near GPU
Under GPU
0927 Change
Near GPU
Under GPU
PLACE CLOSE TO GPU BALLS
Under GPU
Near GPU
Near GPU
Under GPU
Quanta Computer Inc.
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CHANNEL A: 2G/4G GDDR5

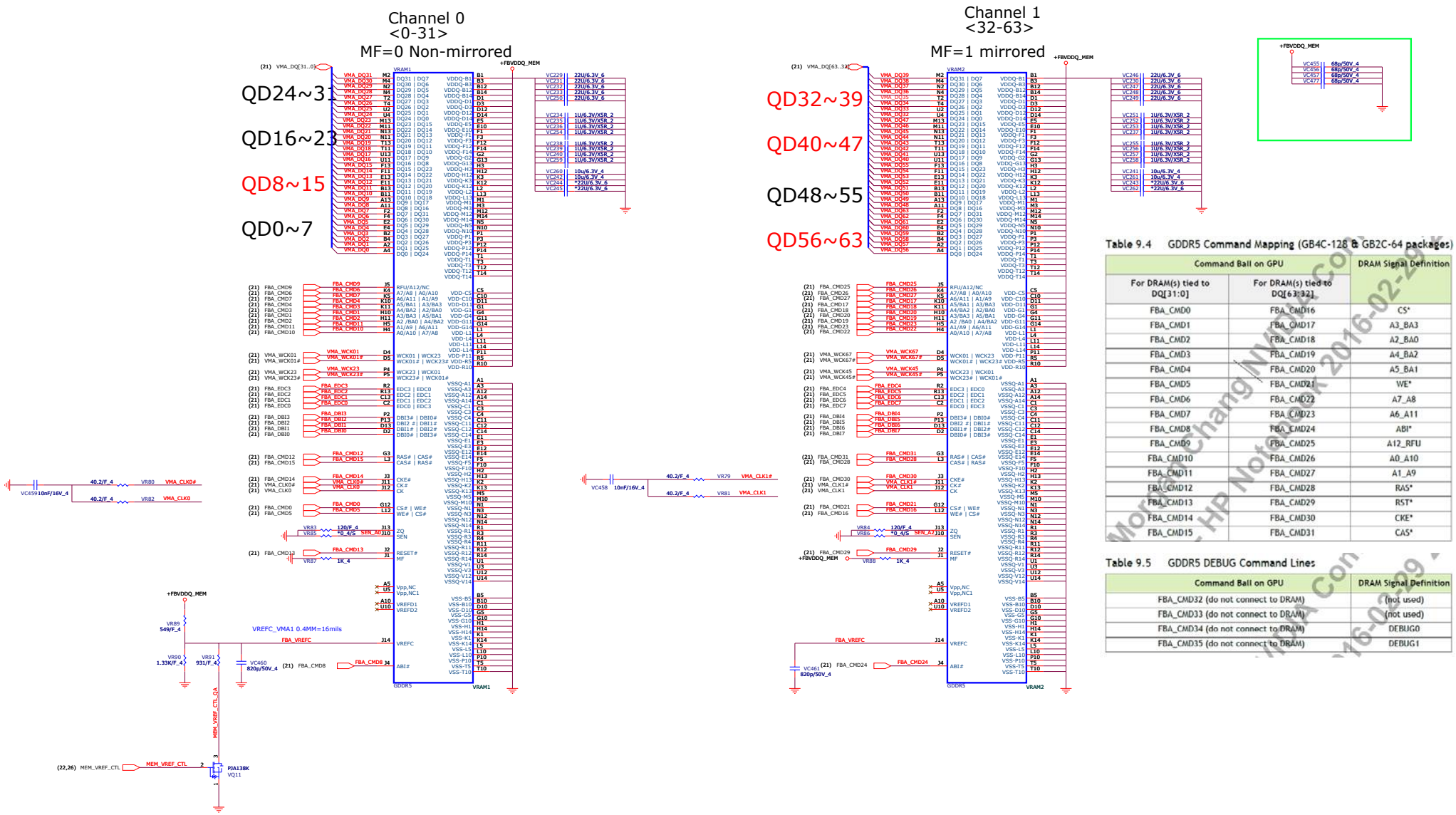


Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

CHANNEL B: 2G/4G GDDR5

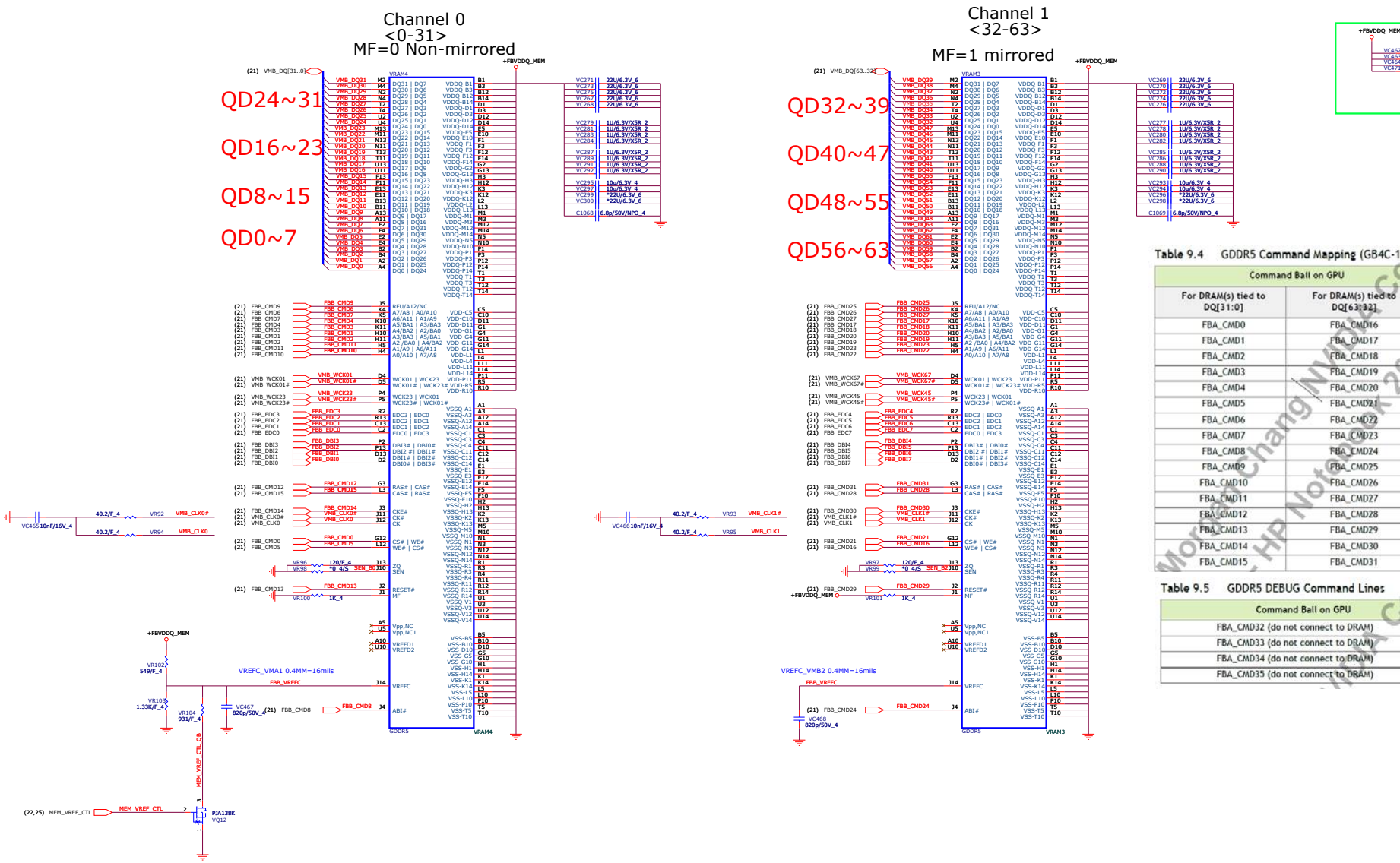


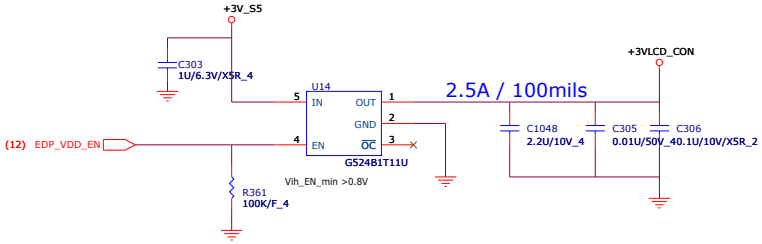
Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

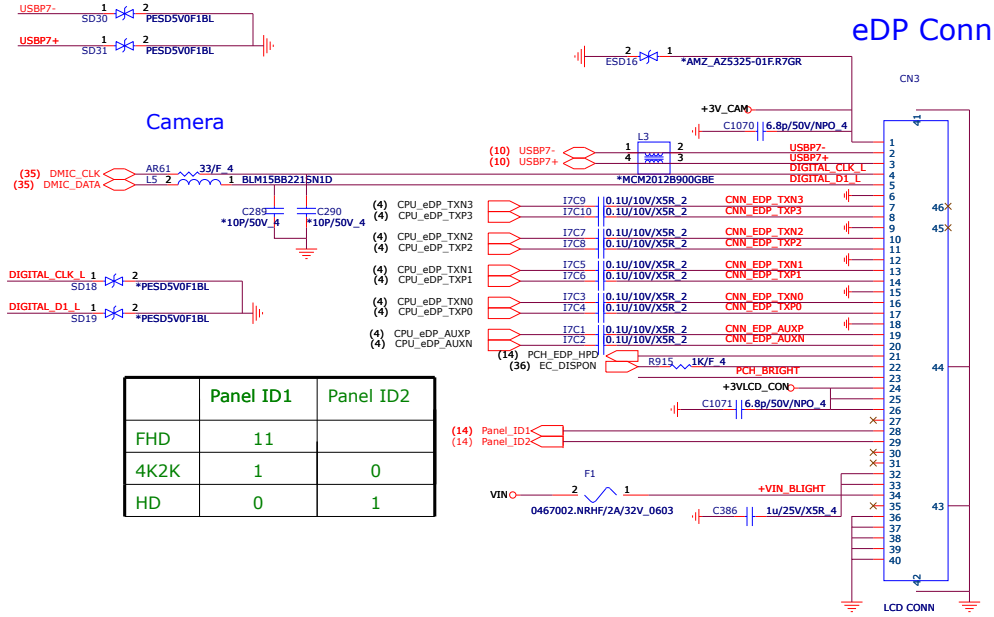
Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

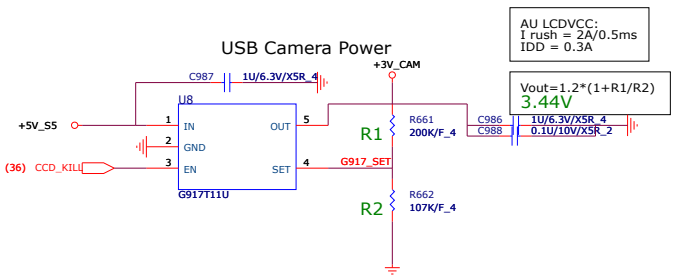
Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

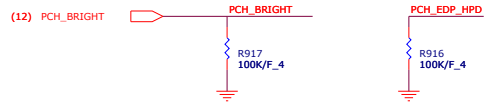
eDP & Camera





	Panel ID1	Panel ID2
FHD	11	
4K2K	1	0
HD	0	1





Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	eDP CONN/CAM/D-MIC	1A

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PROJECT : G35 Quanta Computer Inc.		
Size C	Document Number NA	Rev 1A
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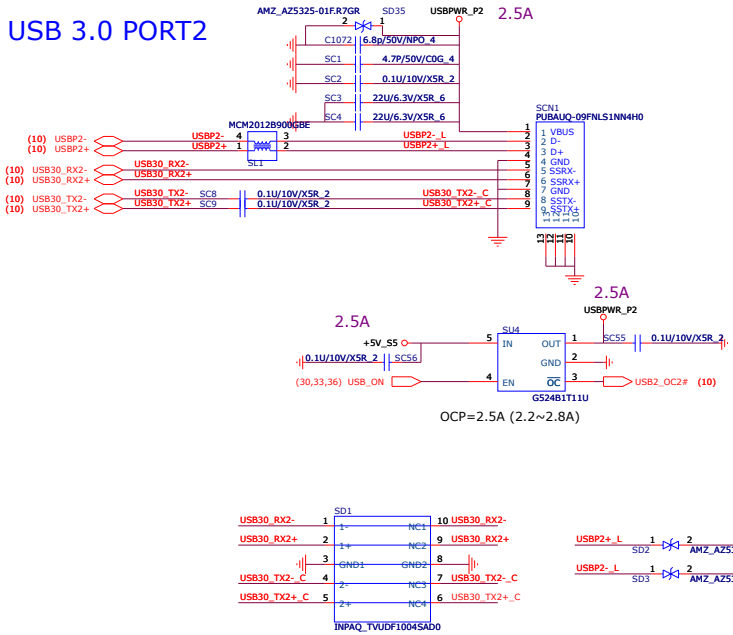
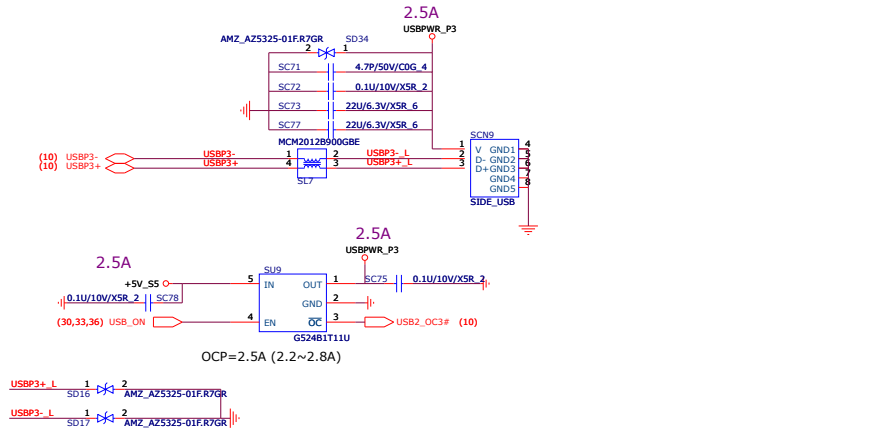
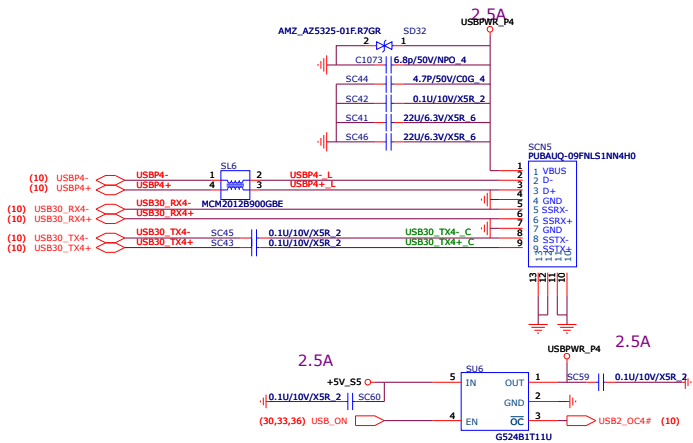
USB 3.0 PORT2



USB 2.0 PORT3

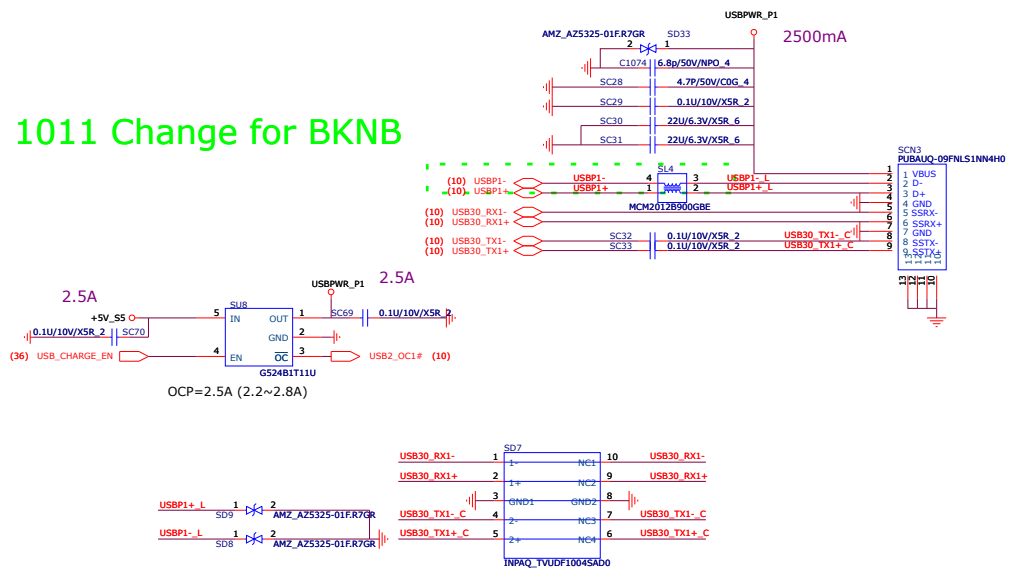


USB 3.0 PORT4



USB 3.0 PORT1

1011 Change for BKNB

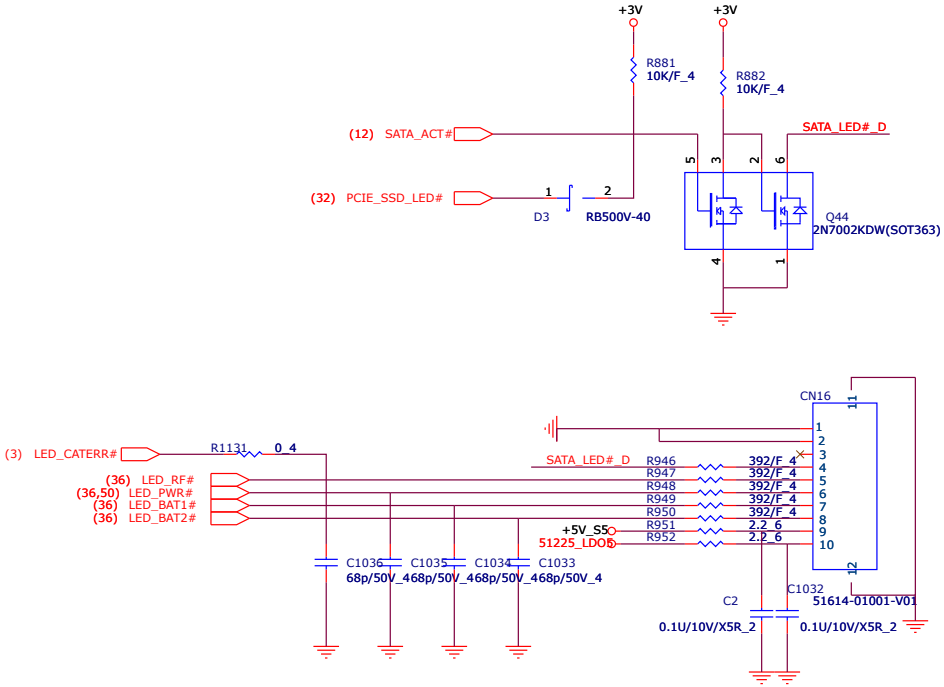


Quanta Computer Inc.
PROJECT : BKLB & BKNB

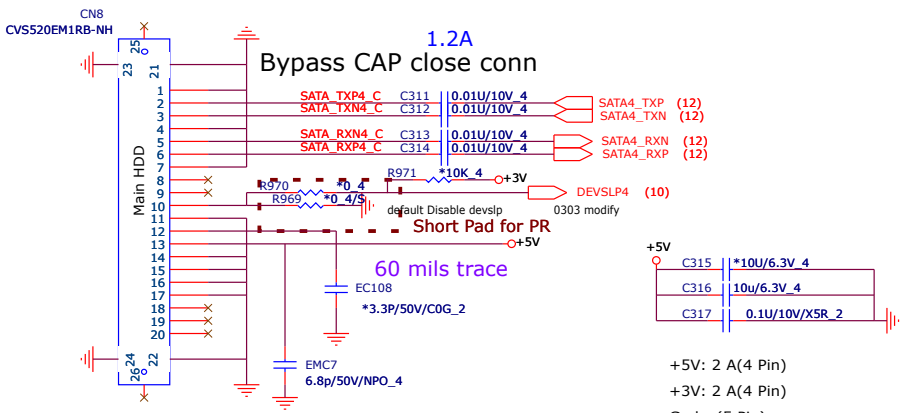
Size	Document Number	Rev
	USB3.0	1A

Date: Tuesday, January 30, 2018 Sheet 30 of 59

LED



SATA HDD Connector(Cable type)



+5V: 2 A(4 Pin)
+3V: 2 A(4 Pin)
Gnd : (5 Pin)

Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	HDD/LED	1A
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SSD

CN10
DFHS75FR322
3.2H

NGFF

+3V_SSD
Max Current : 1.6A(PCIE),1.36A(SATA)

1/4 PR Change
Change 0201 to 0402

+3.3V_ NGFF_WLAN
Max Current : 1000mA

Close to CN10
Short Pad for PR

ngff-apci0020-p002a-75p-km-smt

WLAN/BT

NGFF Wifi/BT (Type E)

DRE(12-0004-01) RDC STD
DFHS75FR026

CN11

NGFF EKEY

+3.3V_ NGFF_WLAN
Max Current : 1000mA

#571483 CRB Schematic
For Glitch Free Operation During Boot Process.
Signals Required Cap or Pull-Down Resistor
3.3V Signaling Mode = 100Kohm
1.8V Signaling Mode = 75Kohm

Follow #571483 CFL-H CRB0.9 Reserve Pull-H Resistor.

Blue Tooth

WIFI

1/4 PR Change
Change 0201 to 0402

Close to CN11

WLAN_NGFF CONN_LTS(APCI0085- P005A)

AC Mode : Support wakle on LAN
DC Mode : Don't support wake on LAN

Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	SSD/WLAN	1A

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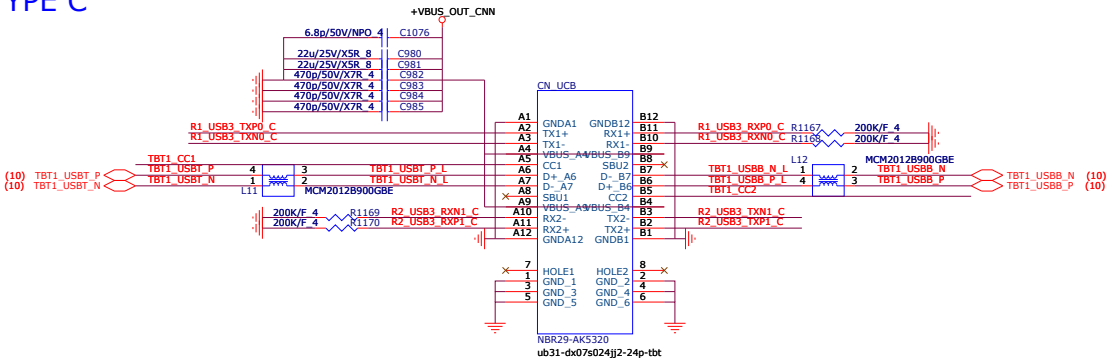
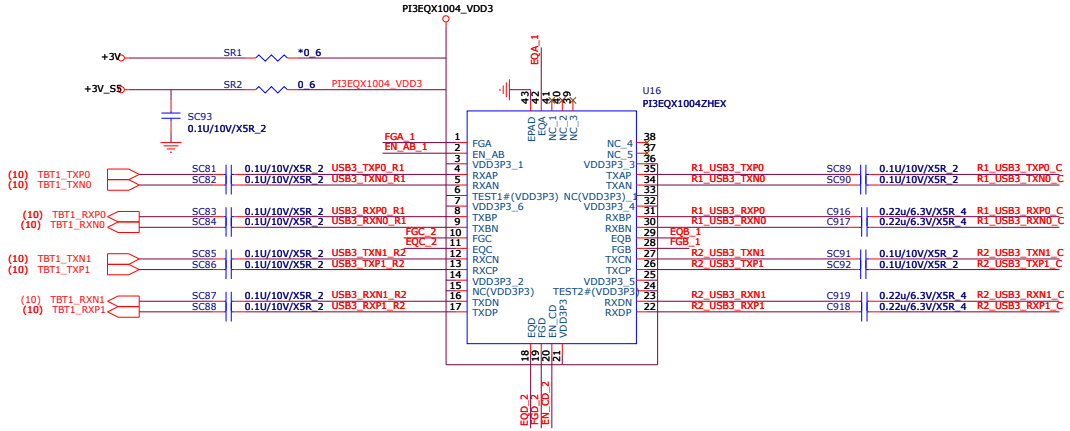
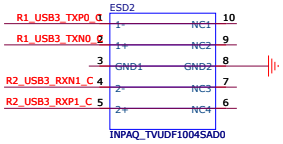
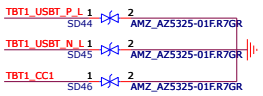
TYPE C

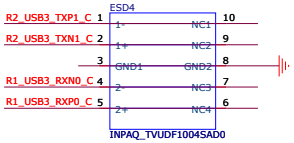
VBUS:5V

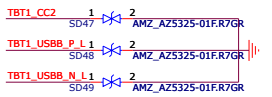


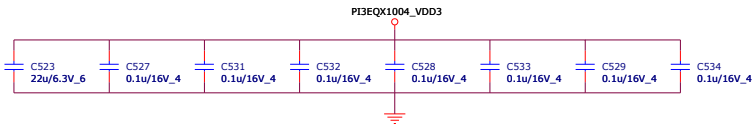












Channel Enable Setting:

EN_AB/EN_CD are the channel enable pins for channels A&B and C&D respectively

	Channel Enable Setting
EN	*Setting*
0	Disabled
1	Enabled (Default)

Equalization Setting:

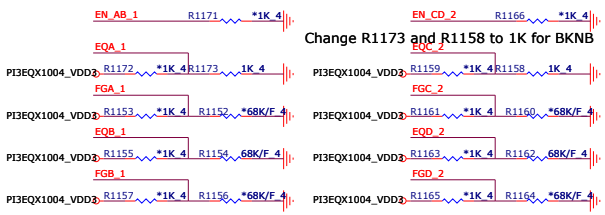
EQA/B/C/D are the selection pins for the equalization selection

	Equalizer setting (dB)	
EQA/B/C/D	*@2.5GHz*	*@5GHz*
0 (Tie 0Ω to GND)	5.1	10.9
R (Tie Rext to GND)	1.9	6.7
F (Leave Open)	3.5	8.9 (Default)
1 (Tie 0Ω to VDD)	6.8	13.1

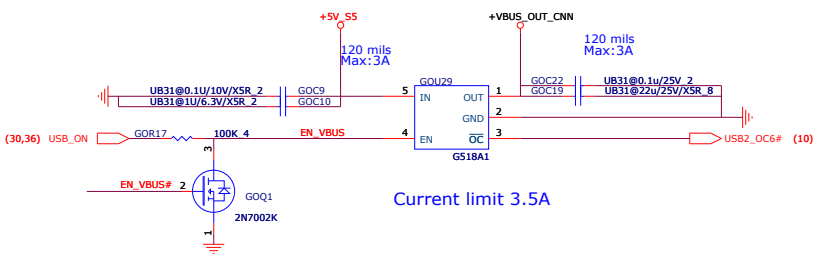
Flat Gain Setting:

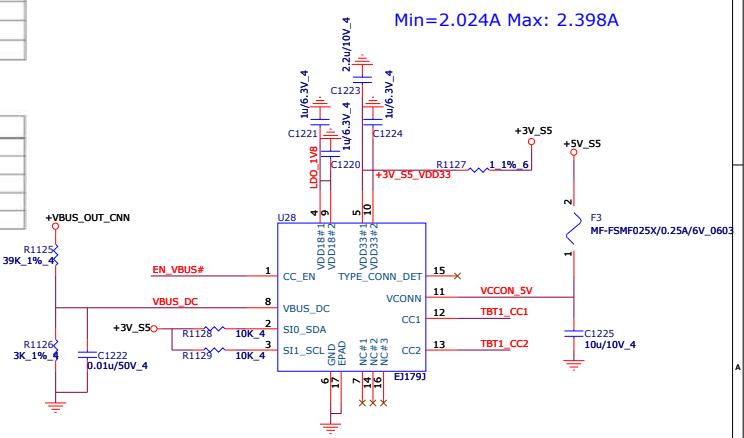
FGA/B/C/D are the selection pins for the DC gain

	Flat Gain Settings
FGA/B/C/D	*dB*
0 (Tie 0Ω to GND)	-3
R (Tie Rext to GND)	-1.5
F (Leave Open)	0 (Default)
1 (Tie 0Ω to VDD)	+2



Change R1173 and R1158 to 1K for BKNB





Size	Document Number	Rev
	USB-C(USB/PD/DP-OUT)	1A
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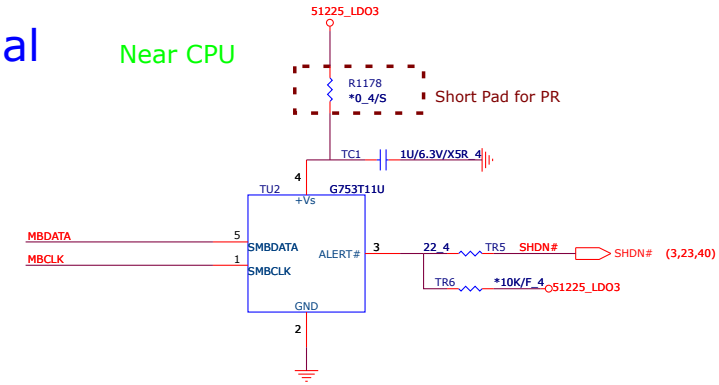
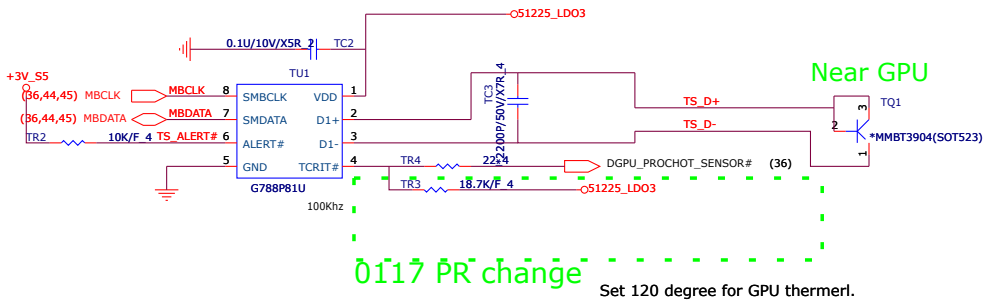
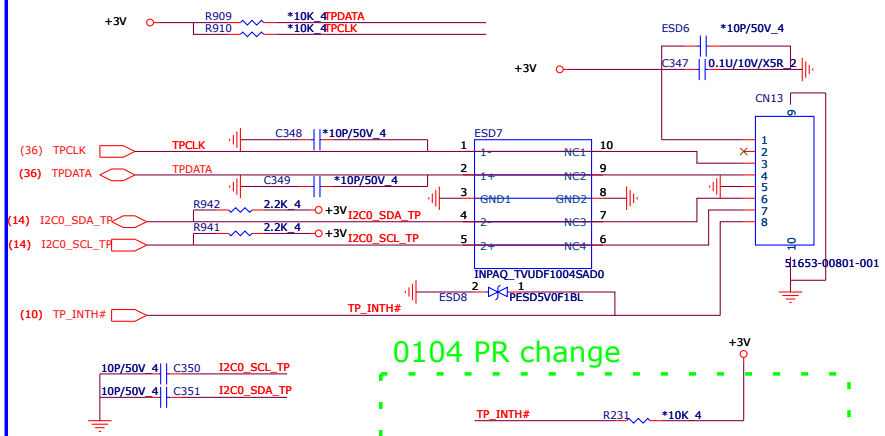
Thermal

Near CPU





Touch Pad Connector AA type



Del R231 10K, because PCH already have 10K

Quanta Computer Inc.			
PROJECT : BKLB & BKNB			
Size	Document Number		Rev
	THM/TP		1A
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Audio Code (ALC295)

0130 PR Change FOR ESD

0110 PR Change FOR ESD

Universal Jack

ALC295

QFN48(6*6)

Thermal pad=DGND

AGND

DGND

Linear regulator

+1.8VA

Digital

Analog

I:0.253A

G9090-18CT11U

S@TAS5766

EC monitor FAULT# to control AMP_MUTE#

Quanta Computer Inc.	
PROJECT : BKLB & BKNB	
Size	Document Number: Audio(ALC295-CG+TAS5766) — Rev 1A
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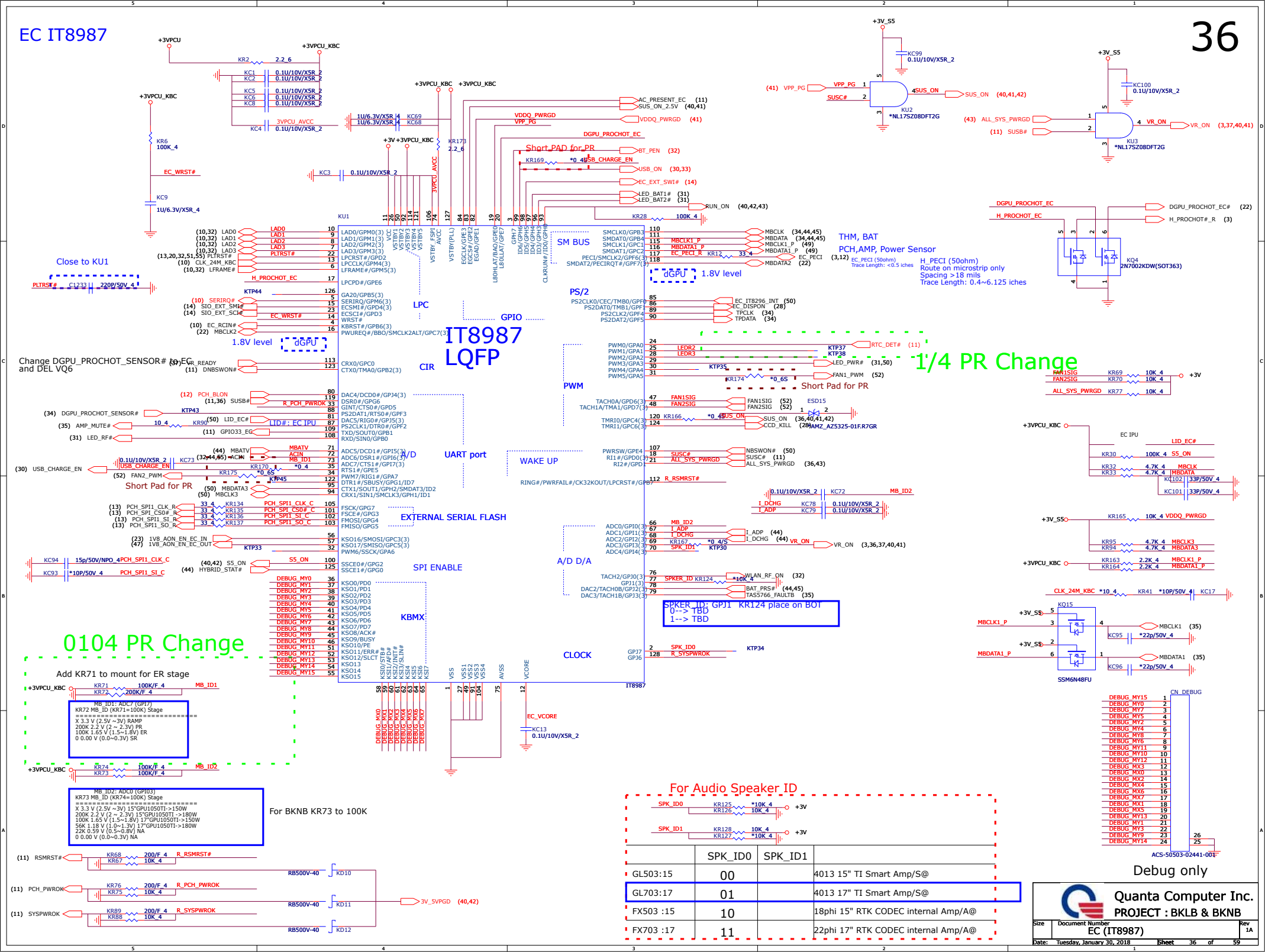
EC IT8987



	SPK_ID0	SPK_ID1	
GL503:15	00		4013 15" TI Smart Amp/S@
GL703:17	01		4013 17" TI Smart Amp/S@
FX503 :15	10		18phi 15" RTK CODEC internal Amp/A@
FX703 :17	11		22phi 17" RTK CODEC internal Amp/A@

Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	EC (IT8987)	1A
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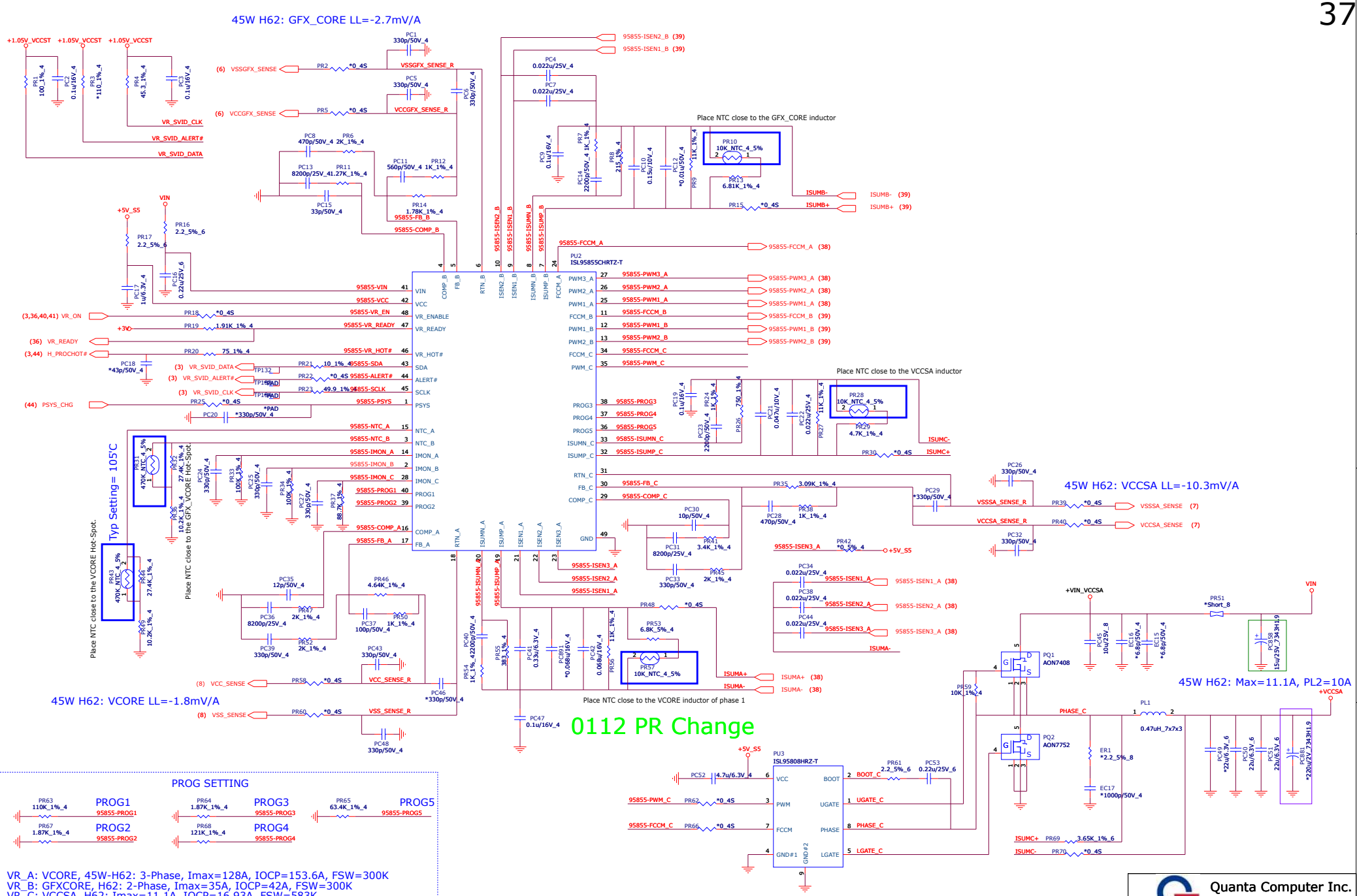

Quanta Computer Inc.
PROJECT : BKLB & BKNB
Size | Document Number: VCCORE/GTCORE/VCCSA (ISL95829A) | Rev 1A
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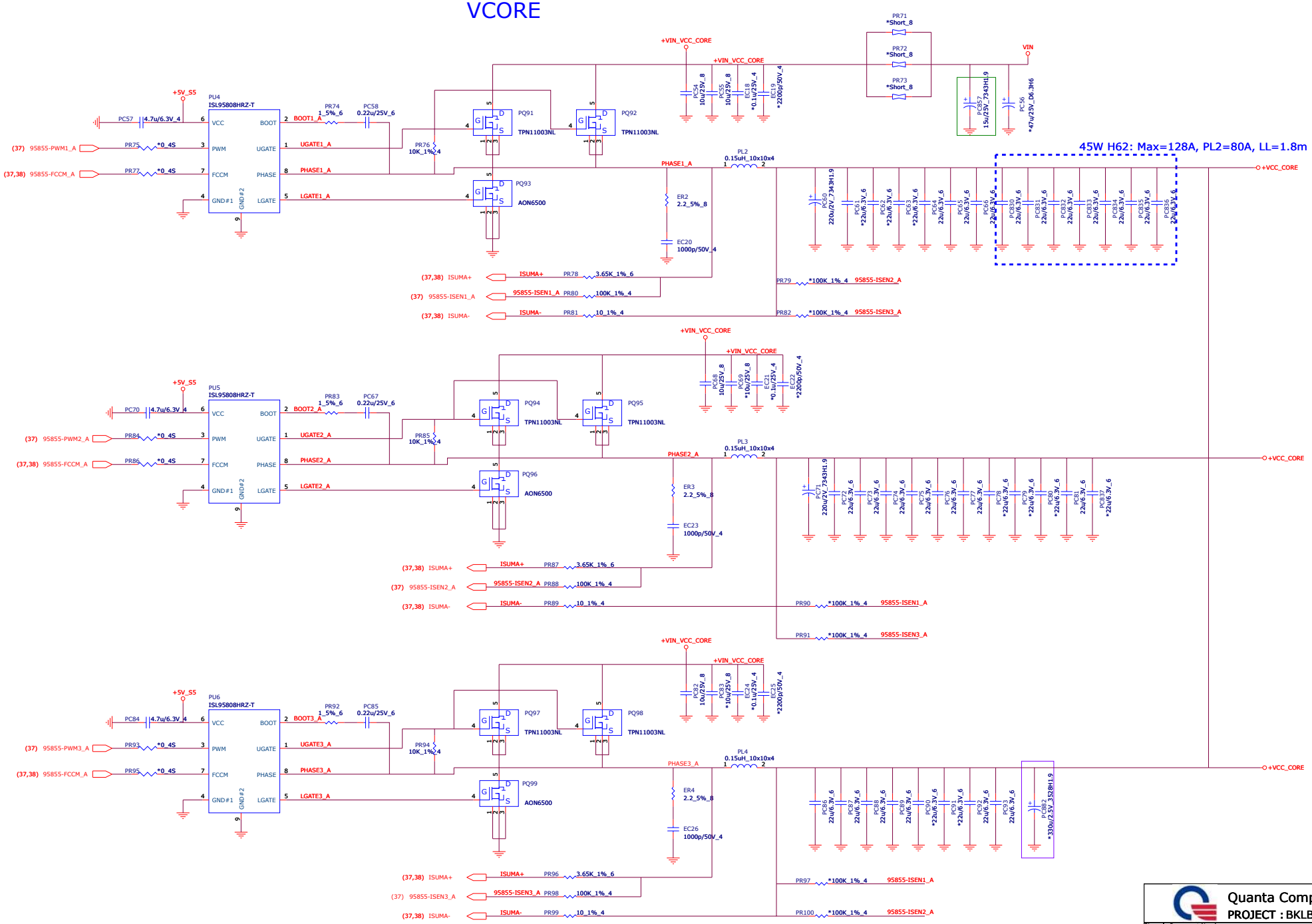
VCORE



Quanta Computer Inc.	
PROJECT : BKLB & BKNB	
Size	Document Number: VCCORE/GTCORE/VCCSA (ISL95829A) Rev: 1A
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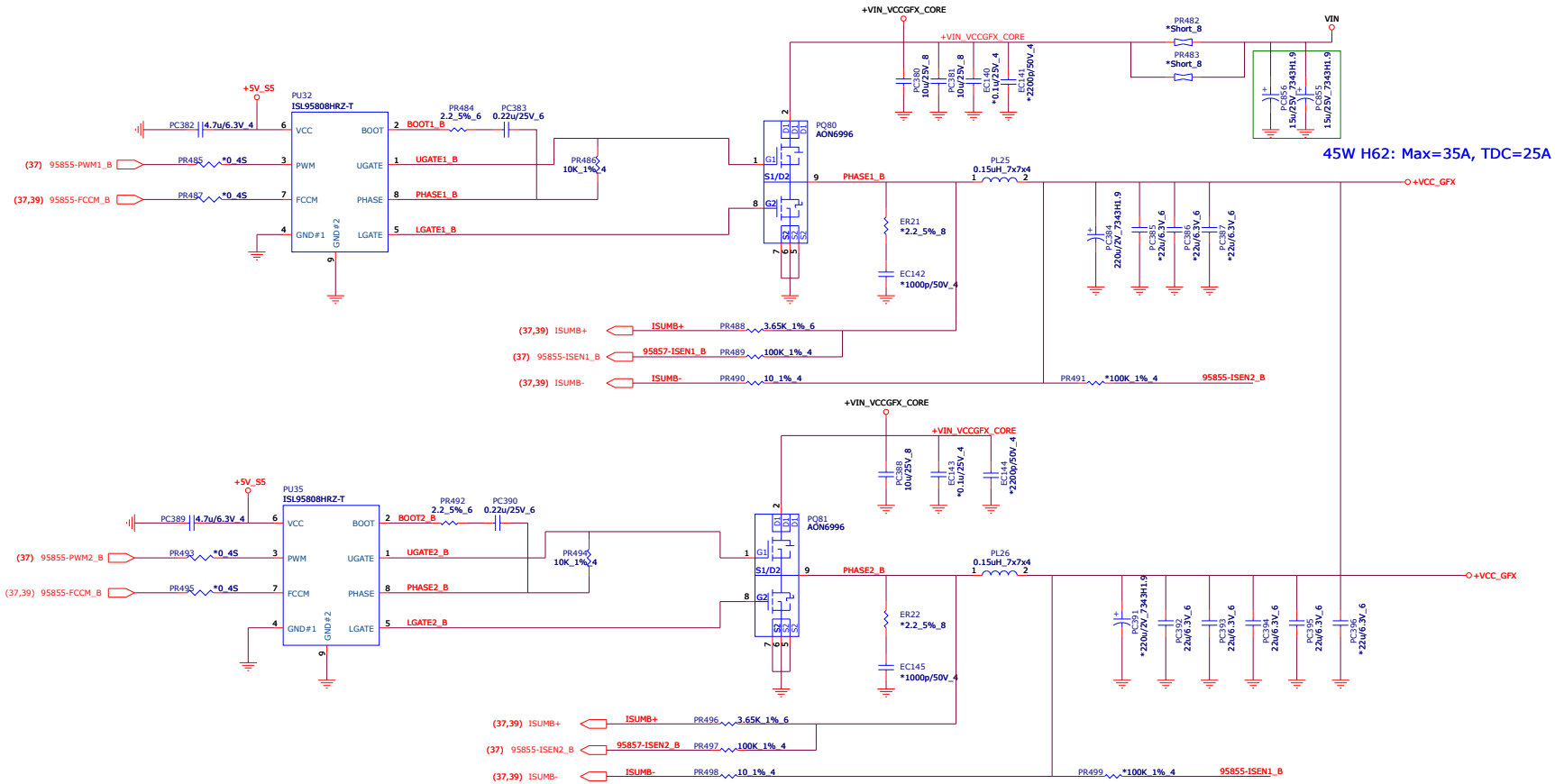
GFX_CORE



Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	GTCORE (ISL95829A)	1A

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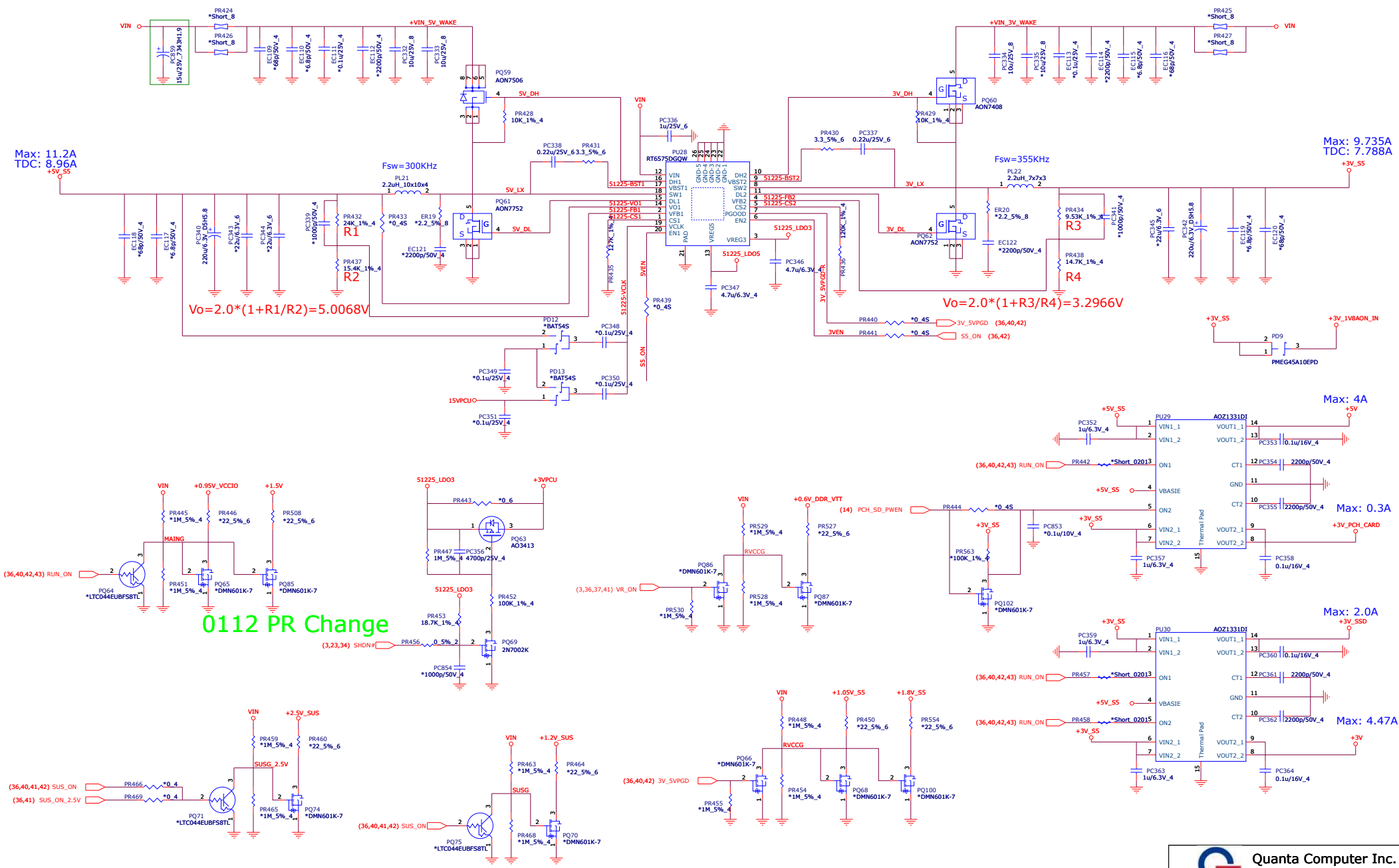
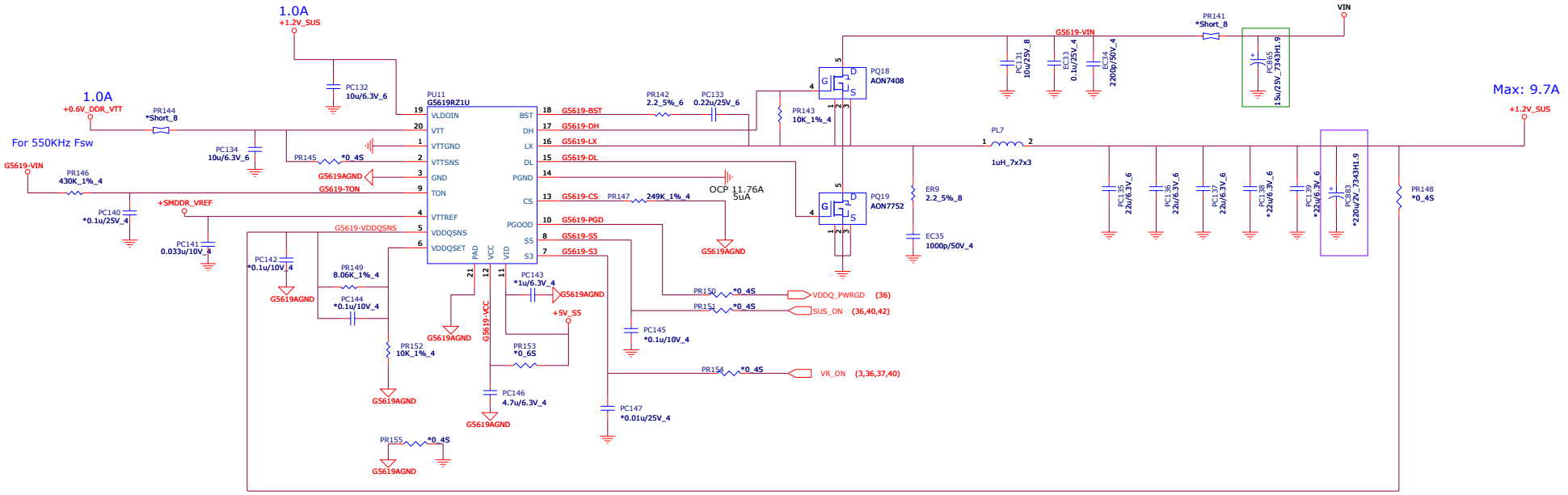
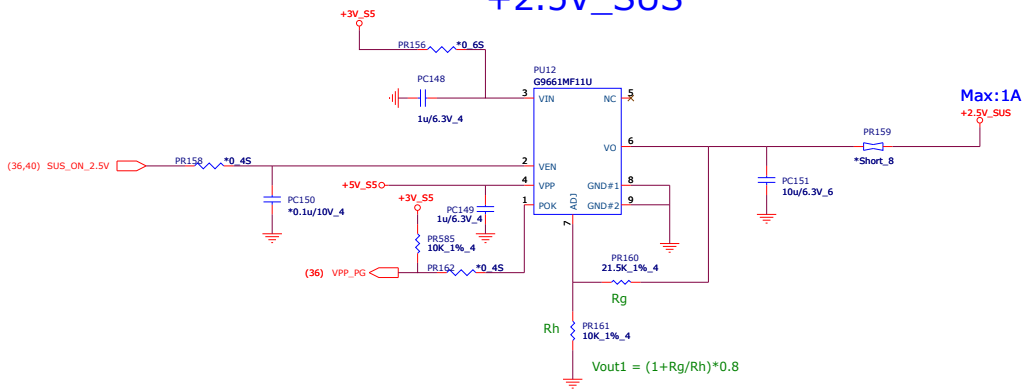

Max: 11.2A
TDC: 8.96A
Fsw=300KHz
Vo=2.0*(1+R1/R2)=5.0068V
R1
R2
Max: 9.735A
TDC: 7.788A
Fsw=355KHz
Vo=2.0*(1+R3/R4)=3.2966V
R3
R4
Max: 4A
Max: 0.3A
Max: 2.0A
Max: 4.47A
0112 PR Change
RT6575DGQW
AON7506
AON7408
AON7752
AO3413
2N7002K
AOZ1331DI
PMEG45A10EPD

1.2VSUS & VTT_MEM



STATE	S3	S5	1.35VSUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	00		Off	Off	Off

+2.5V_SUS



Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	1.2VSUS/VTT_MEM	1A
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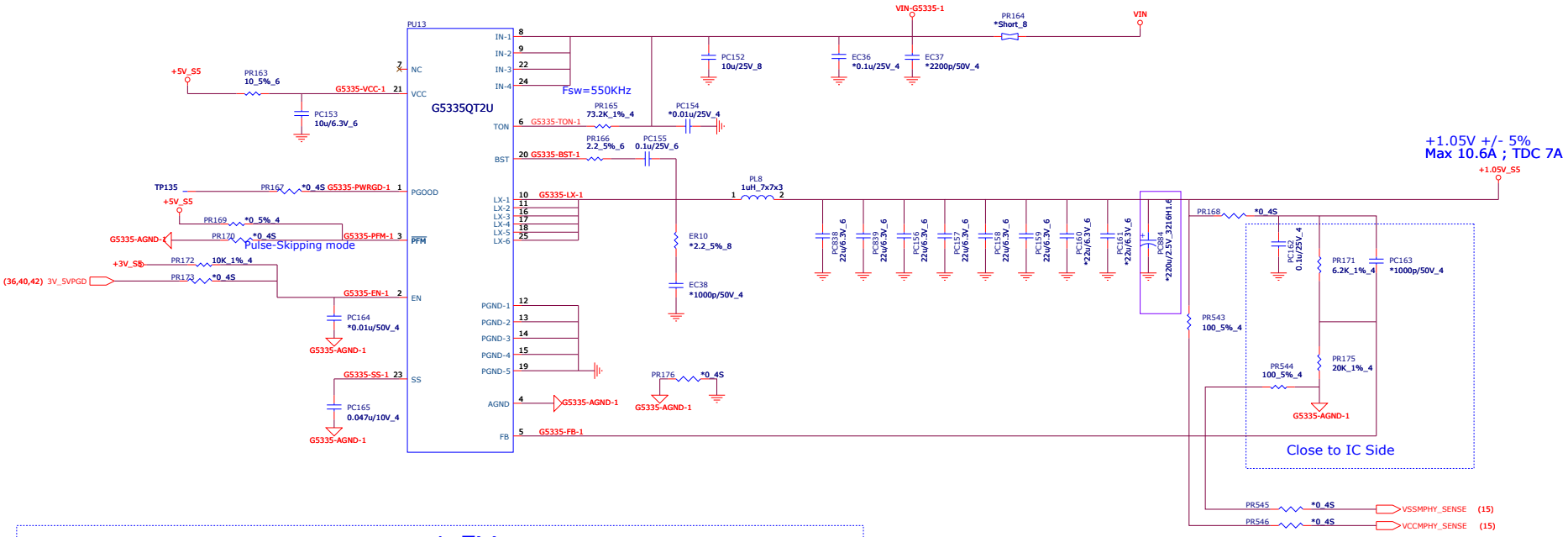
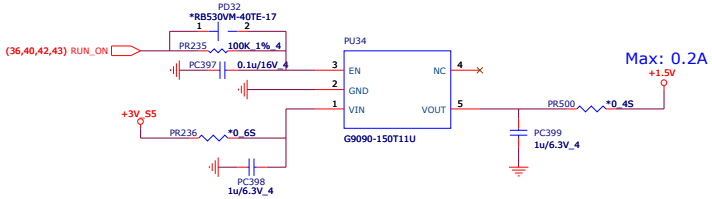
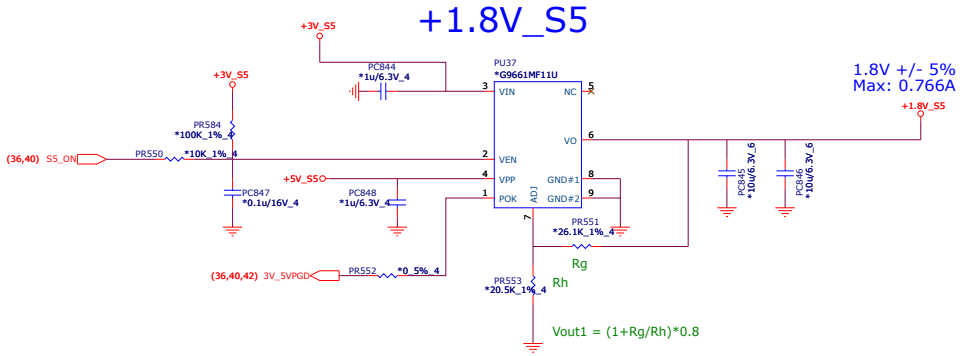
+1.05V_S5

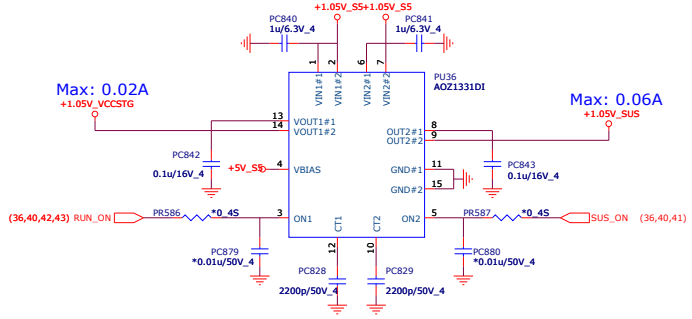


+1.5V



+1.8V_S5





Quanta Computer Inc.
PROJECT : BKLB & BKNB

Size	Document Number	Rev
	+1.0V_S5 / +1.5V	1A
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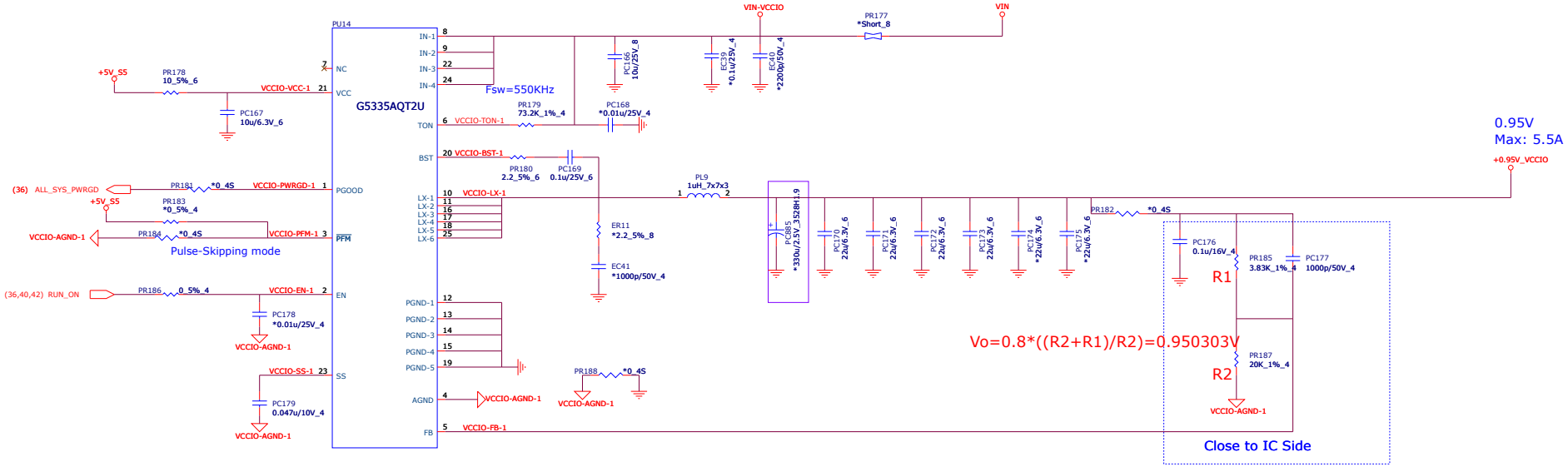
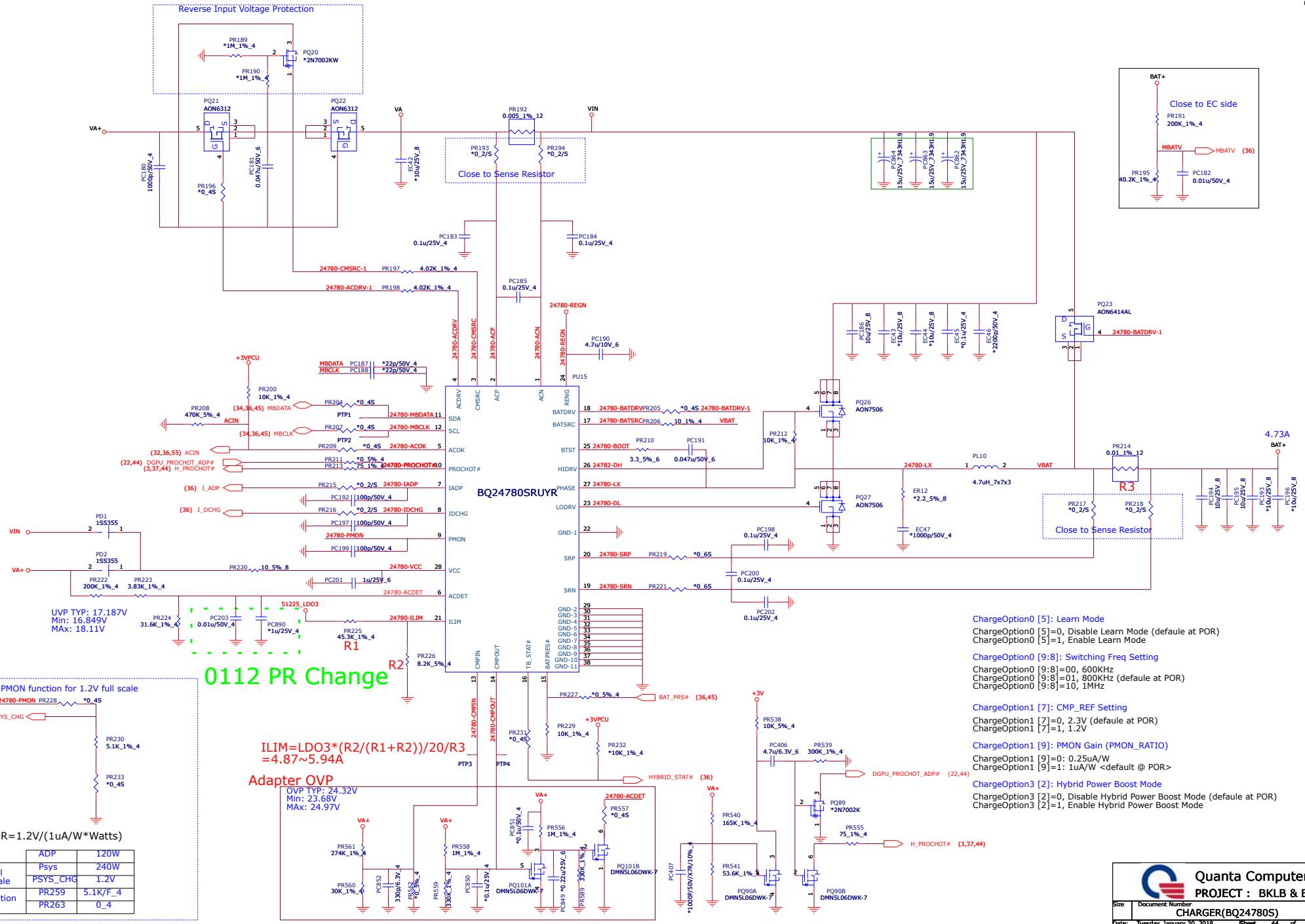
+VCCIO (Fix VCCIO=0.95V)




Reverse Input Voltage Protection
PR189 *1M_1%_4
PR190 *1M_1%_4
PQ20 *2N7002KW
PQ21 AON6312
PQ22 AON6312
VA+
VA
VIN
PR192 0.005_1%_12
PR193 *0_2/S
PR194 *0_2/S
Close to Sense Resistor
PC180 1000p/50V_4
PC181 0.047u/50V_6
PR196 *0_4S
EC42 *10u/25V_8
PC183 0.1u/25V_4
PC184 0.1u/25V_4
PC185 0.1u/25V_4
PC190 4.7u/10V_6
24780-CMSRC-1
24780-ACDRV-1
PR197 4.02K_1%_4
PR198 4.02K_1%_4
24780-REGN
+3VPCU
MBDATA PC187 *22p/50V_4
MBCLK PC188 *22p/50V_4
PR200 10K_1%_4
PR208 470K_5%_4
ACIN
PR204 *0_4S
PR207 *0_4S
PR209 *0_4S
PR211 *0_5%_4
PR213 75_1%_4
PR215 *0_2/S
PR192 100p/50V_4
PR216 *0_2/S
PR197 100p/50V_4
PR199 100p/50V_4
PR220 10_5%_8
PC201 1u/25V_6
PR222 200K_1%_4
PR223 3.83K_1%_4
PR224 31.6K_1%_4
PC203 0.01u/50V_4
PC890 *1u/25V_4
51225_LDO3
PR225 45.3K_1%_4
R1
PR226 8.2K_5%_4
R2
0112 PR Change
PD1 1SS355
PD2 1SS355
UVP TYP: 17.187V
Min: 16.849V
MAx: 18.11V
PU15
BQ24780SRUYR
ACDRV
CMSRC
ACP
ACN
REGN
BATDRV
BATSRC
BTST
HIDRV
PHASE
LODRV
GND-1
SRP
SRN
SDA
SCL
ACOK
PROCHOT#
IADP
IDCHG
PMON
VCC
ACDET
ILIM
CMPIN
CMPOUT
TB_STAT#
BATPRES#
24780-BATDRV
24780-BATSRC
24780-BOOT
24782-DH
24780-LX
24780-DL
24780-SRP
24780-SRN
24780-MBDATA
24780-MBCLK
24780-ACOK
24780-PROCHOT#
24780-IADP
24780-IDCHG
24780-PMON
24780-VCC
24780-ACDET
24780-ILIM
24780-CMPIN
24780-CMPOUT
PR205 *0_4S 24780-BATDRV-1
PR206 10_1%_4 VBAT
PR210 3.3_5%_6
PR191 0.047u/50V_6
PQ26 AON7506
PQ27 AON7506
PR212 10K_1%_4
ER12 *2.2_5%_8
EC47 *1000p/50V_4
PL10 4.7uH_7x7x3
24780-LX
VBAT
PR214 0.01_1%_12
R3
PR217 *0_2/S
PR218 *0_2/S
Close to Sense Resistor
4.73A
BAT+
PC186 10u/25V_8
EC43 *10u/25V_8
EC44 *10u/25V_8
EC45 *0.1u/25V_4
EC46 *2200p/50V_4
PQ23 AON6414AL
24780-BATDRV-1
PC198 0.1u/25V_4
PC200 0.1u/25V_4
PC202 0.1u/25V_4
PR219 *0_6S
PR221 *0_6S
PC194 10u/25V_8
PC195 10u/25V_8
PC193 *10u/25V_8
PC196 *10u/25V_8
PR227 *0_5%_4
BAT_PRS# (36,45)
PR231 *0_4S
PR229 10K_1%_4
PR232 *10K_1%_4
+3V
PR538 10K_5%_4
PC406 4.7u/6.3V_6
PR539 300K_1%_4
DGPU_PROCHOT_ADP# (22,44)
PQ89 *2N7002K
PR555 75_1%_4
H_PROCHOT# (3,37,44)
PR540 165K_1%_4
PR541 53.6K_1%_4
PC407 *1000P/50V/X7R/10%_4
PQ90A DMN5L06DWK-7
PQ90B DMN5L06DWK-7
HYBRID_STAT# (36)
ILIM=LDO3*(R2/(R1+R2))/20/R3
=4.87~5.94A
Adapter OVP
OVP TYP: 24.32V
Min: 23.68V
MAx: 24.97V
PR561 274K_1%_4
PR560 30K_1%_4
PC852 330p/6.3V_4
PR558 1M_1%_4
PR559 330K_1%_4
PC850 *0.1u/25V_4
PC851 *0.1u/50V_4
PR556 1M_1%_4
PQ101A DMN5L06DWK-7
PR557 *0_4S
PQ101B DMN5L06DWK-7
PC849 *0.22u/25V_6
PR849 330K_1%_4
PR849 *0_5%_4
PTP1
PTP2
PTP3
PTP4
PMON function for 1.2V full scale
24780-PMON PR228 *0_4S
(37) PSYS_CHG
PR230 5.1K_1%_4
PR233 *0_4S
R=1.2V/(1uA/W*Watts)
Full Scale
ADP 120W
Psys 240W
Location
PSYS_CHG 1.2V
PR259 5.1K/F_4
PR263 0_4
BAT+
Close to EC side
PR191 200K_1%_4
MBATV
MBATV (36)
PR195 40.2K_1%_4
PC182 0.01u/50V_4
ChargeOption0 [5]: Learn Mode
ChargeOption0 [5]=0, Disable Learn Mode (defaule at POR)
ChargeOption0 [5]=1, Enable Learn Mode
ChargeOption0 [9:8]: Switching Freq Setting
ChargeOption0 [9:8]=00, 600KHz
ChargeOption0 [9:8]=01, 800KHz (defaule at POR)
ChargeOption0 [9:8]=10, 1MHz
ChargeOption1 [7]: CMP_REF Setting
ChargeOption1 [7]=0, 2.3V (defaule at POR)
ChargeOption1 [7]=1, 1.2V
ChargeOption1 [9]: PMON Gain (PMON_RATIO)
ChargeOption1 [9]=0: 0.25uA/W
ChargeOption1 [9]=1: 1uA/W <default @ POR>
ChargeOption3 [2]: Hybrid Power Boost Mode
ChargeOption3 [2]=0, Disable Hybrid Power Boost Mode (defaule at POR)
ChargeOption3 [2]=1, Enable Hybrid Power Boost Mode
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PROJECT : BKLB & BKNB
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CHARGER(BQ24780S)
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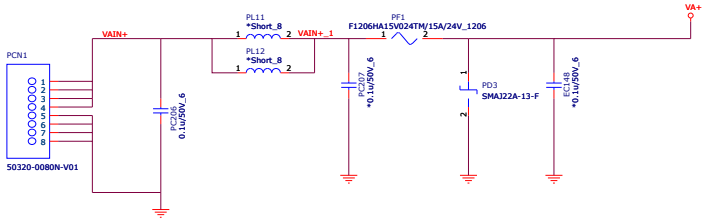
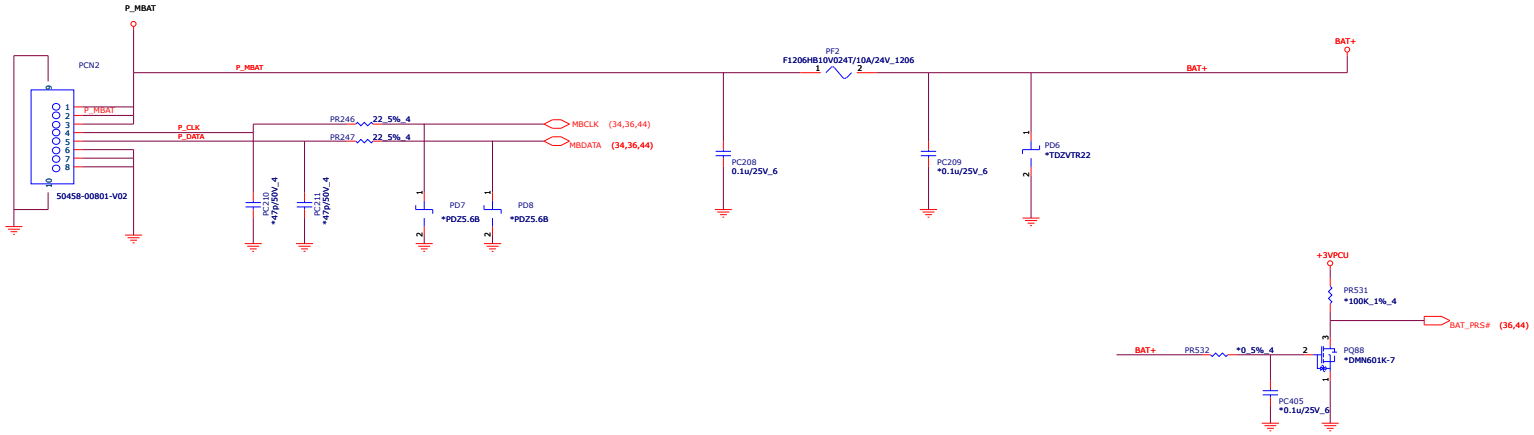
AC IN

AC ADAPTOR IN CONN



BAT IN



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Size	Document Number	Rev
	ADP IN / BAT IN / Thermal Protection	1A

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+NVVDD

N17P-G0 (TDP=40W)
Max=100A, TDC=50A
N17P-G1 (TDP=50W)
Max=124A, TDC=59A

0112 PR Change

Fsw setting=300KHZ

OpenVreg Type2+

OC setting with 10uA source
G0 OCP Min 120A
G1 OCP Min 140A

GPU_PSI Status:

PSI Voltage	Operating Phase Number
0V~0.4V	1 phase with DEM
0.8V~1V	1 phase with CCM
1.4V~5.5V	Active phase with CCM (Only for 2 or 3 hases)

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PROJECT : BKLB & BKNB
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FBVDDQ - 1.5V_GPU

0112 PR Change

Fsw Setting=430KHz

OC Setting

1.35V / 1.55V
MAX: 20A, TDC:11A

FBVDDQ Voltage Setting: 1.55V / 1.35V

FBVDDQ_CTRL	PR353	PR354	FBVDDQ
1	12K	3.57K	1.55V
0	12K	3.57K	1.35V

FBVDDQ Voltage Setting: 1.50V / 1.35V

FBVDDQ_CTRL	PR353	PR354	FBVDDQ
1	12.4K	2.94K	1.50V
0	12.4K	2.94K	1.35V

R1

R2

VOUT=(1+R1/R2)*0.7

Load Switch for GPU

0112 PR Change

1.6A

1.0V
Max: 1.1A

Discharge

+1.0V_GPU

1.0V
Max: 1.1A

Rg

Rh

Vout1 = (1+Rg/Rh)*0.8

+1.8V_GPU_AON

Max: 1.8A
TDC: 1.0A

Rg

Rh

Vout1 = (1+Rg/Rh)*0.8

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Size	Document Number	Rev
	+FBVDDQ (G5318)	1A

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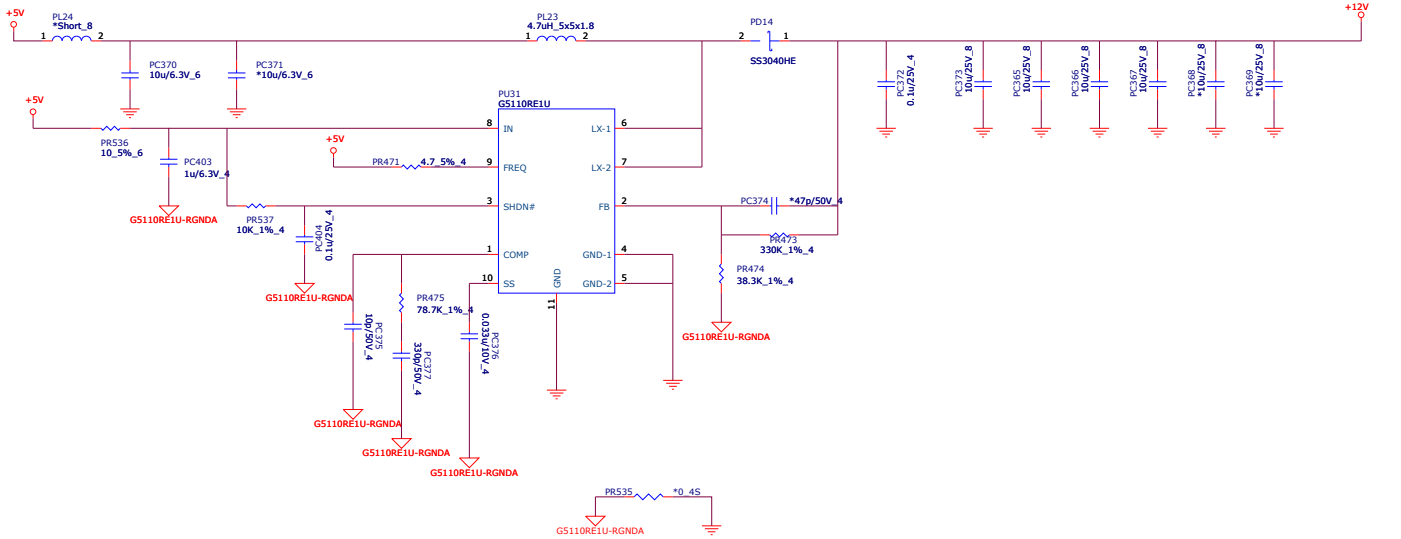
+12V for FAN

Max 1.4A



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PROJECT : BKLB & BKNB		
Size	Document Number: +1.0V_VCCEDRAM / +12V	Rev: 1A
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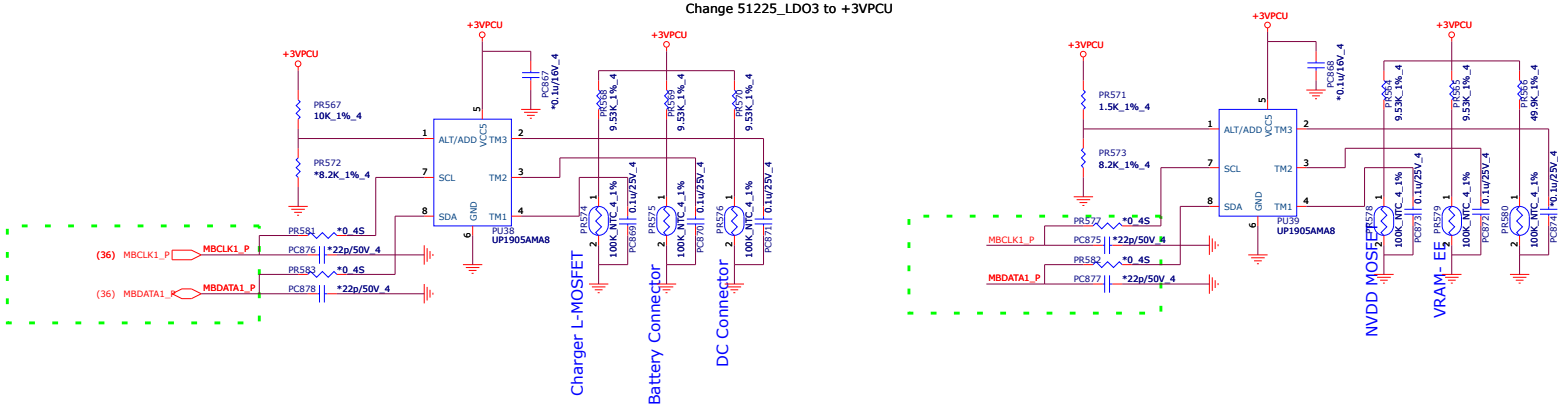
Change 51225_LDO3 to +3VPCU



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Size	Document Number	Rev
		1A

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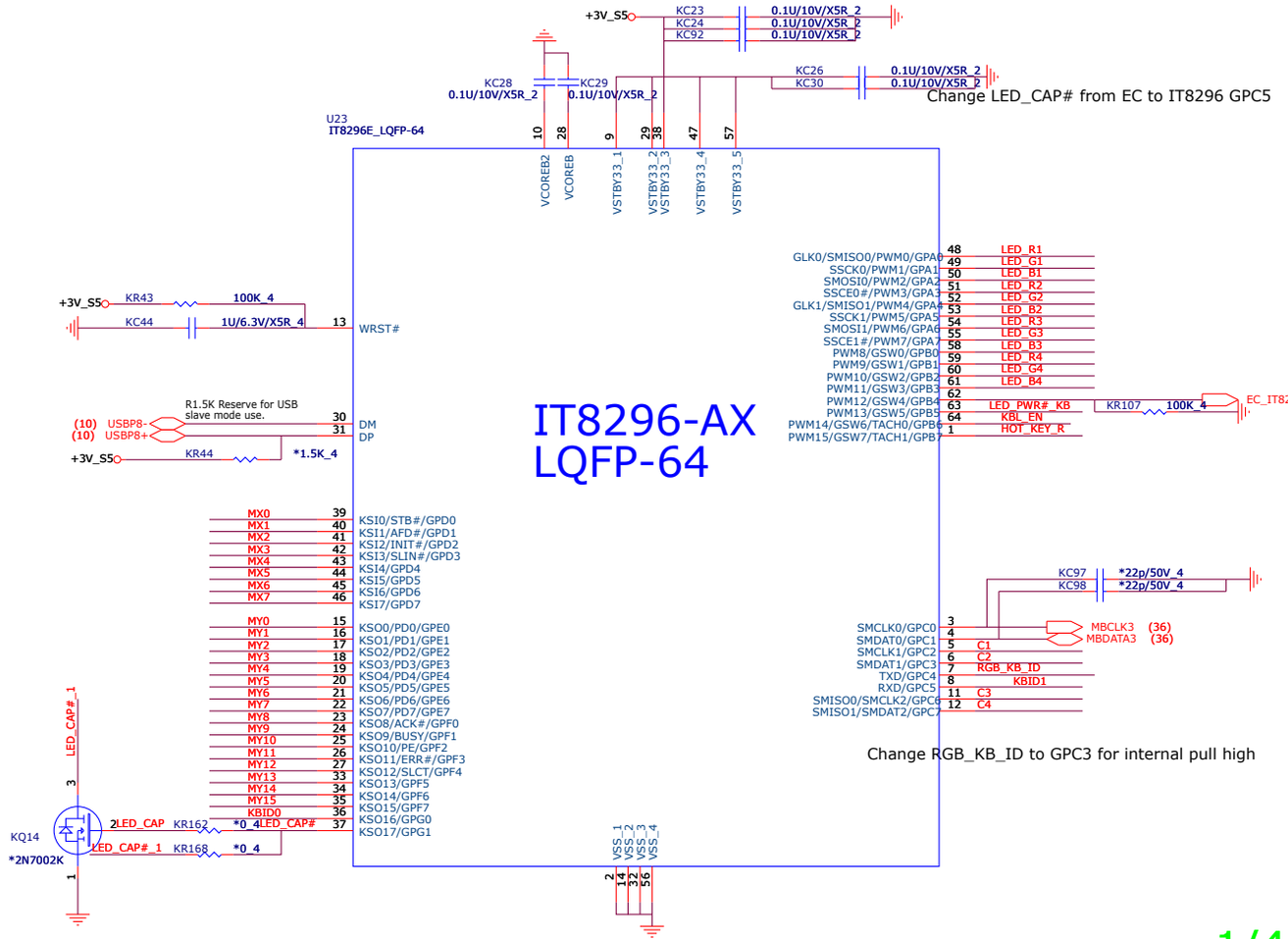
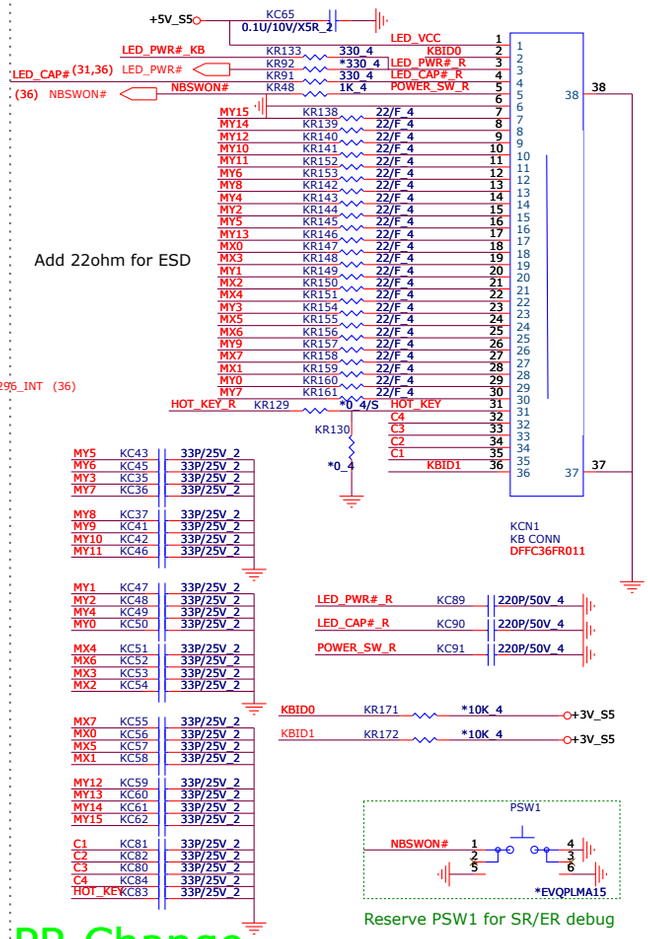
ANTI Ghost with LED driver



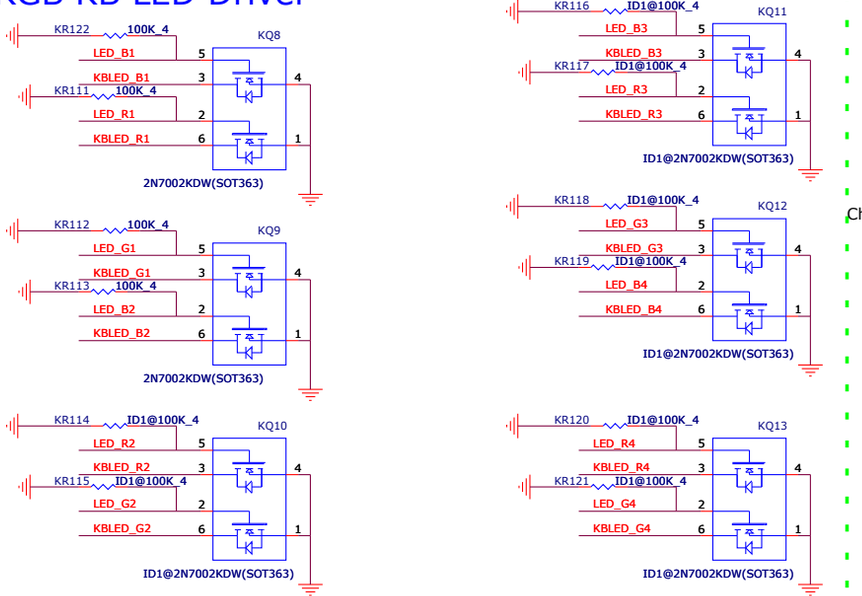
KEYBOARD Con.

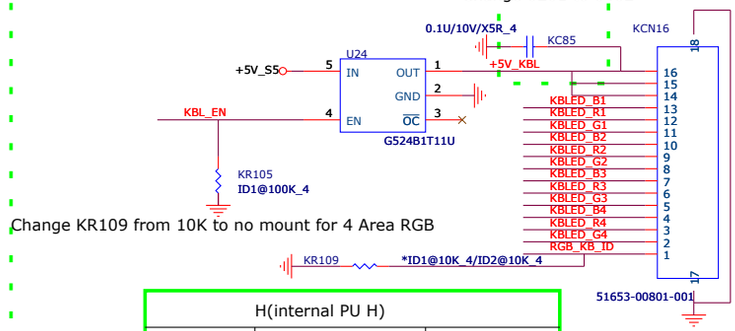


1/4 PR Change

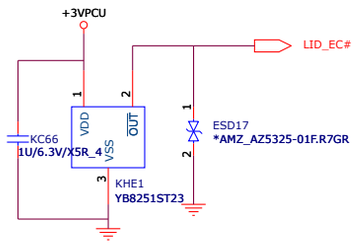
Change 0201 to 0402

RGB KB LED Driver





H(internal PU H)		
	4 Area RGB	1 Area R
KR109	No mount	Mount



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Size	Document Number	Rev
	EC(IT8296)	1A
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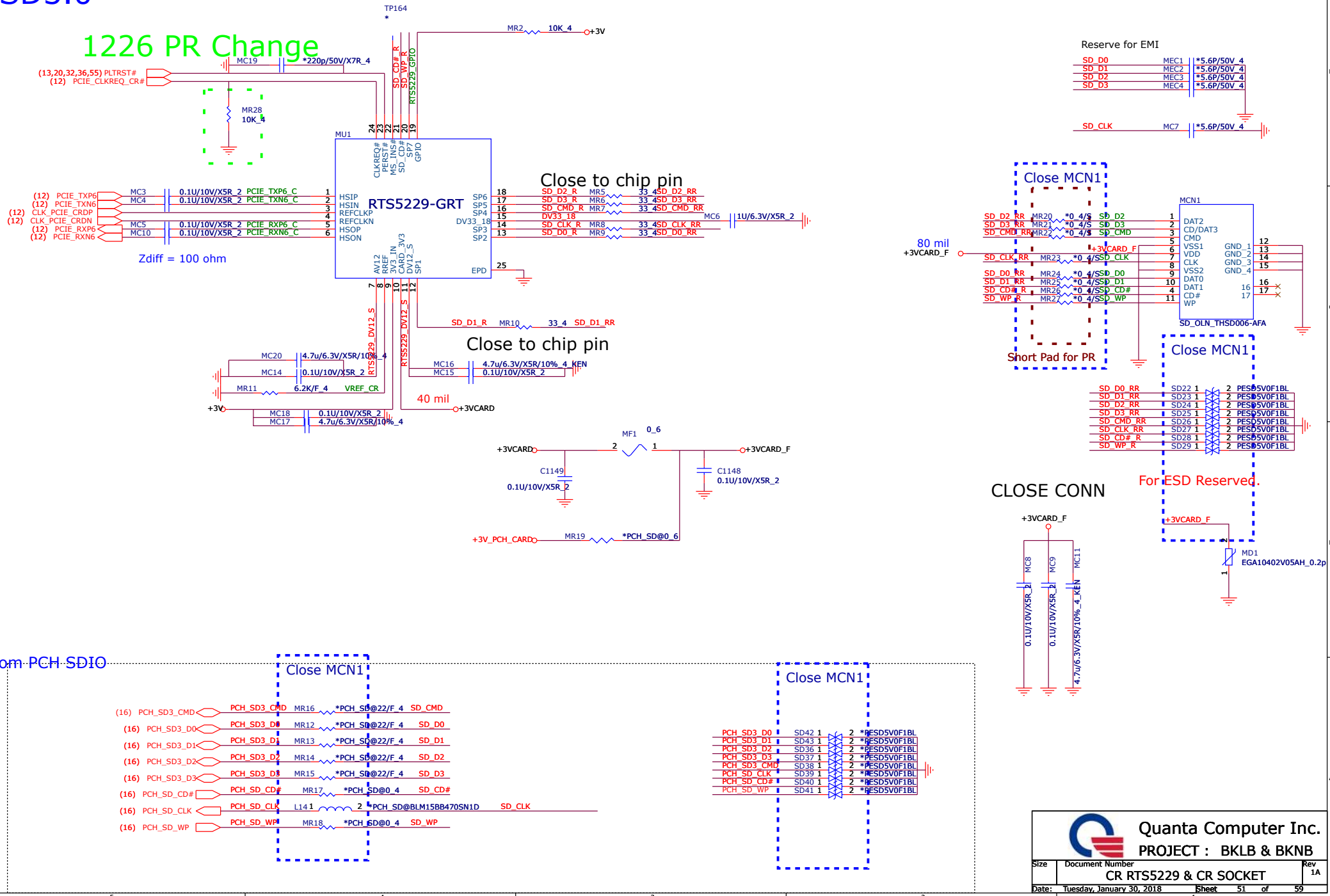
SD3.0

1226 PR Change



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Size	Document Number	Rev
	CR RTS5229 & CR SOCKET	1A
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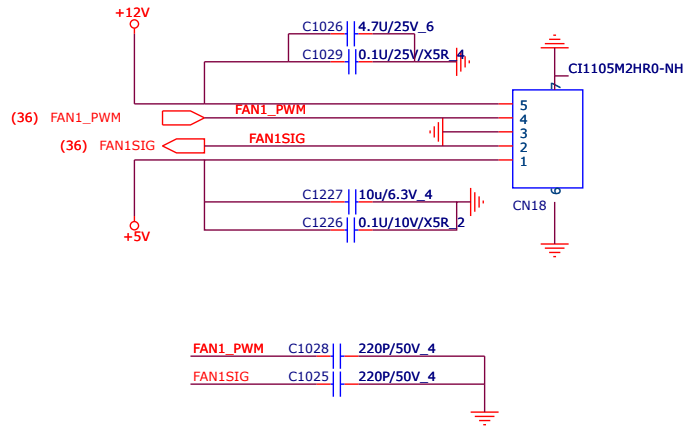
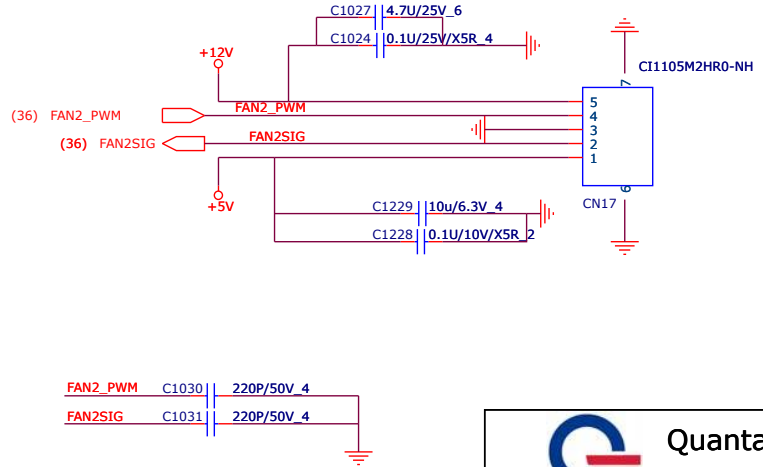
FAN1 for GPU



FAN2 for CPU



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	FAN	1A
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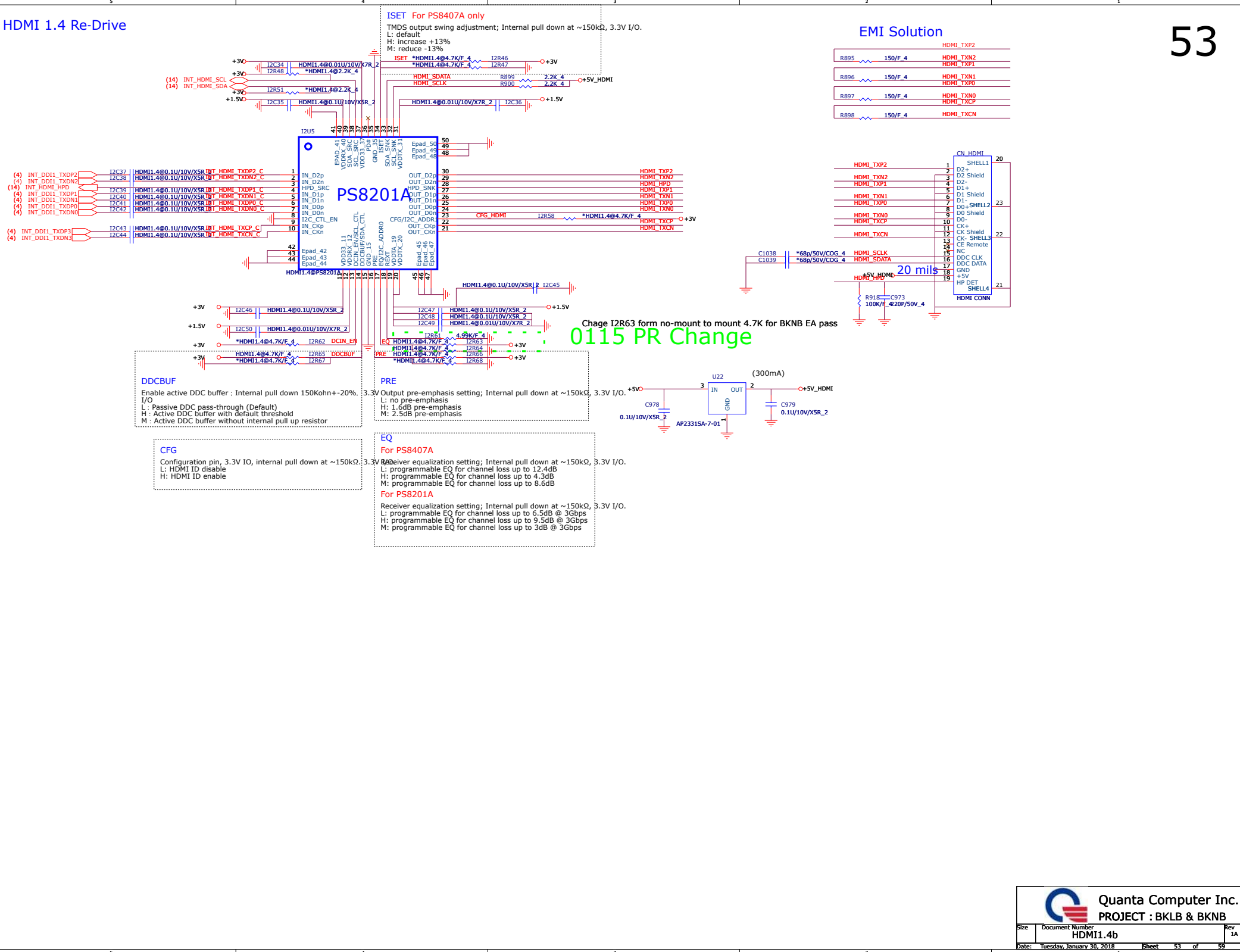
HDMI 1.4 Re-Drive



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Size	Document Number		Rev
	HDMI1.4b		1A
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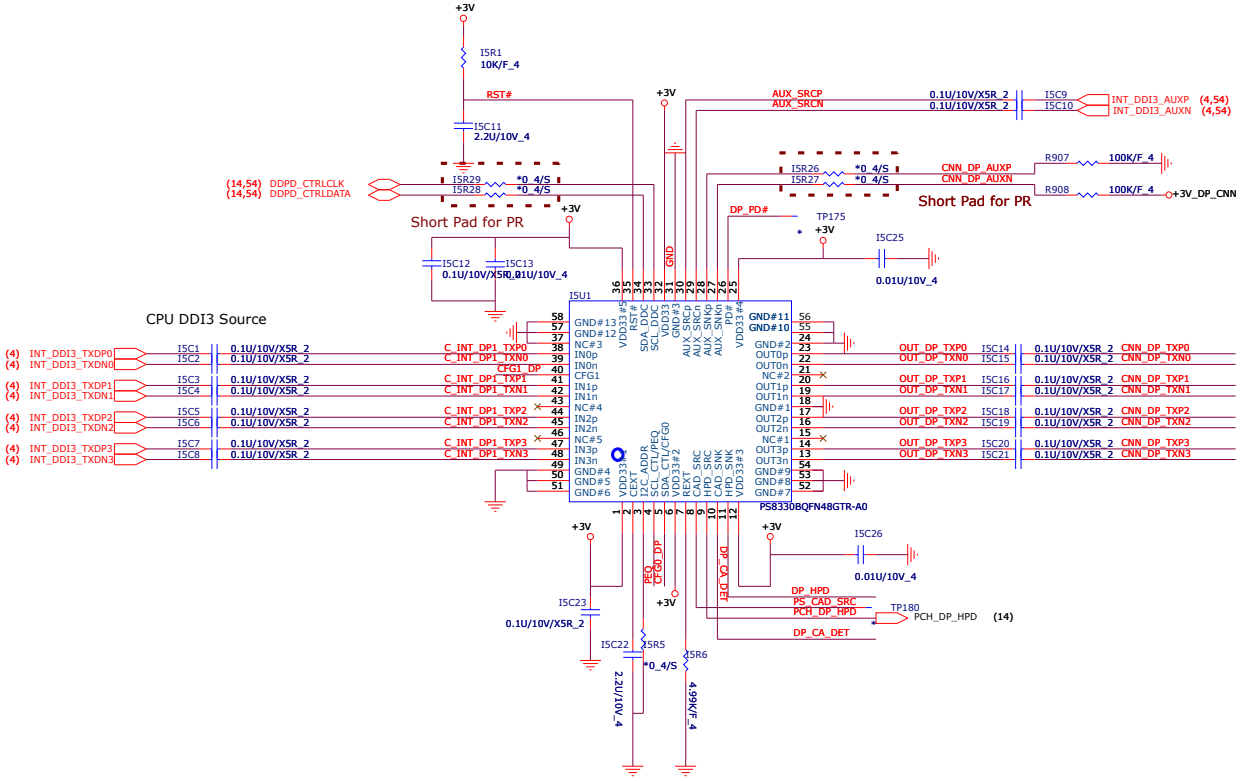
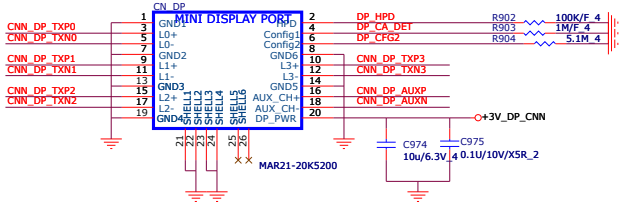
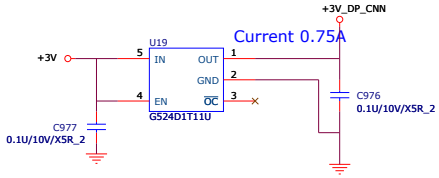
Dual-Mode DisplayPort (DP++)

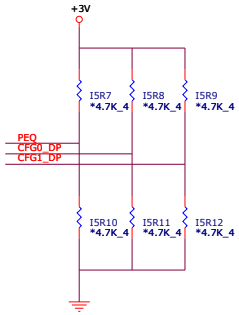


Mini-DP





PS8330 strap pin



PEQ
Programmable input equalization levels; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2

CFG0_DP
Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

CFG1_DP
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K
H: default, auto test disable & input offset cancellation enable
L: auto test enable & input offset cancellation enable
M: auto test disable & input offset cancellation disable

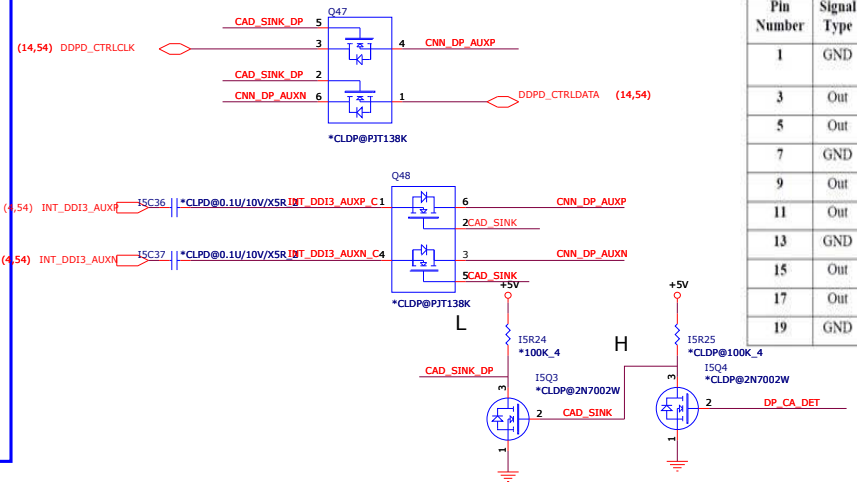


Table 2-1: Source-Side Mini DisplayPort Connector Pin Assignment

Top Row			Bottom Row		
Pin Number	Signal Type	Pin Name	Pin Number	Signal Type	Pin Name
1	GND	GND	2	In	Hot Plug Detect
3	Out	ML_Lane 0 (p)	4	CONFIG (see note 1)	CONFIG1
5	Out	ML_Lane 0 (n)	6	CONFIG (see note 1)	CONFIG2
7	GND	GND	8	GND	GND
9	Out	ML_Lane 1 (p)	10	Out	ML_Lane 3 (p)
11	Out	ML_Lane 1 (n)	12	Out	ML_Lane 3 (n)
13	GND	GND	14	GND	GND
15	Out	ML_Lane 2 (p)	16	I/O	AUX_CH (p)
17	Out	ML_Lane 2 (n)	18	I/O	AUX_CH (n)
19	GND	GND	20	PWR Out (see note 2)	DP_PWR

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PROJECT : BKLB & BKNB			
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	Mini-DP/Re-driver		1A
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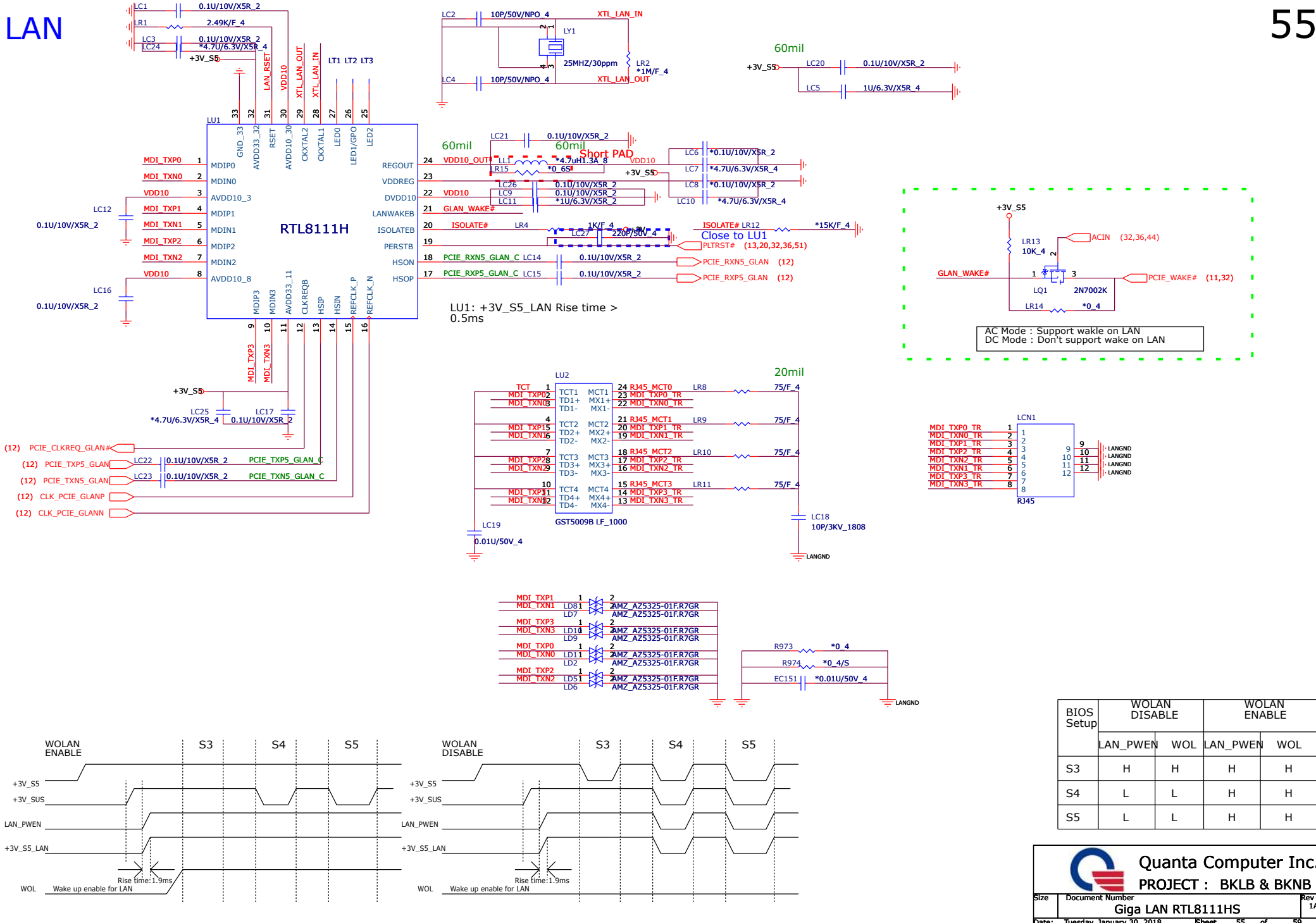
LAN



BIOS Setup	WOLAN DISABLE		WOLAN ENABLE	
	LAN_PWEN	WOL	LAN_PWEN	WOL
S3	H	H	H	H
S4	L	L	H	H
S5	L	L	H	H

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	Giga LAN RTL8111HS	1A
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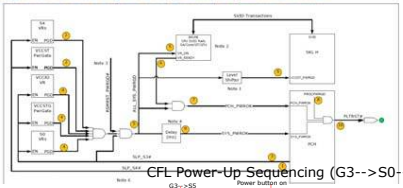
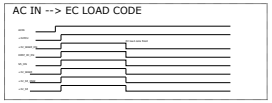
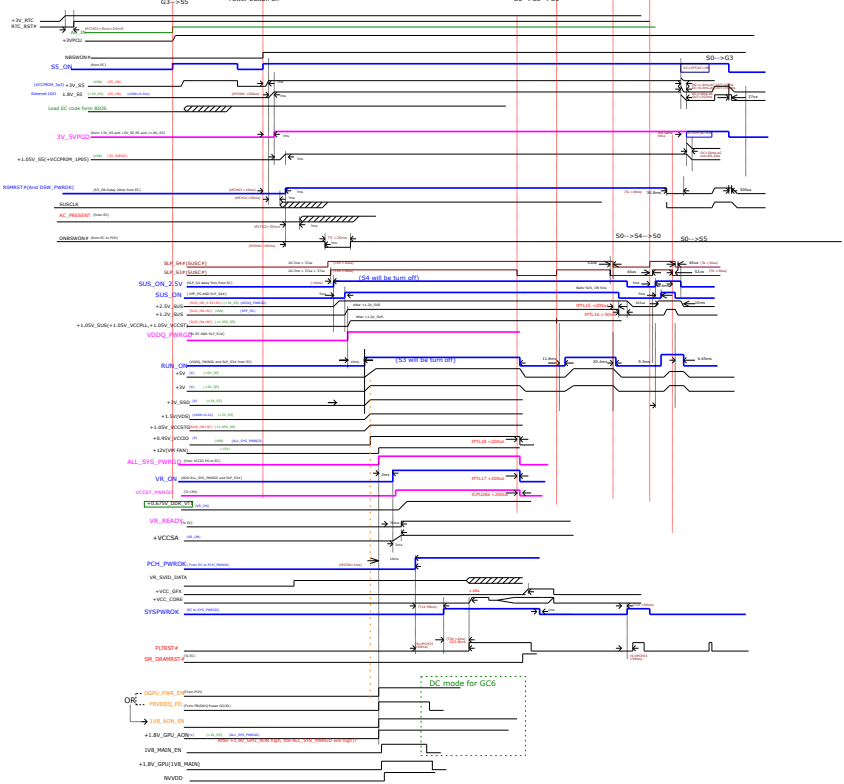
Figure 45-1. CFL Flow Diagram for SYS_PWROK/PCH_PWROK Generation



AC IN --> EC LOAD CODE



CFL Power-Up Sequencing (G3-->S0+->S3-->S4-->S5)



OS status	S0	S3		(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)	
H/W status	S0	S3		S4 (Win10 off) RTC wake Enable WOLAN Enable	S4 (Win10 off) RTC wake Disable WOLAN Disable	S5 (Fast Startup "v")	S5 (Fast Startup "x")	
RUN_ON	HL			L	L	L	L	
+3V	HL			L	L	L	L	
+5V	HL			L	L	L	L	
+0.675V_DDR_VTT	HL			L	L	L	L	
+12V	HL			L	L	L	L	
+3V_SSD/+3V_PCH_CARD/+1.5V	HL			L	L	L	L	
+1.05V_VCCSTG	HL			L	L	L	L	
+VCCSA	HL			L	L	L	L	
+VCC_GFX	HL			L	L	L	L	
+VCC_CORE	HL			L	L	L	L	
+0.95V_VCCIO	HL			L	L	L	L	
SUS_ON	HH			L	LL	L		
+1.05V_VCCPLL/+1.05V_VCCST	H	H		L	L	L	L	
+1.05V_SUS	HH			L	L	L	L	
+1.2V_SUS	H	H		L	L	L	L	
SUS_ON_2.5V	H	H		L	L	L	L	
+2.5V_SUS	H	H		L	L	L	L	
S5_ON	HL	H		H	L		L	
+1.8V_S5	H	H		HL	L		L	
+1.05V_S5	H	H		H	L	L	L	
S5_ON	H	H		H	L	H	L	
+3V_S5	H	H		H	L	H	L	
+5V_S5	HH	H		H	L		L	

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	POWER MAP	1A

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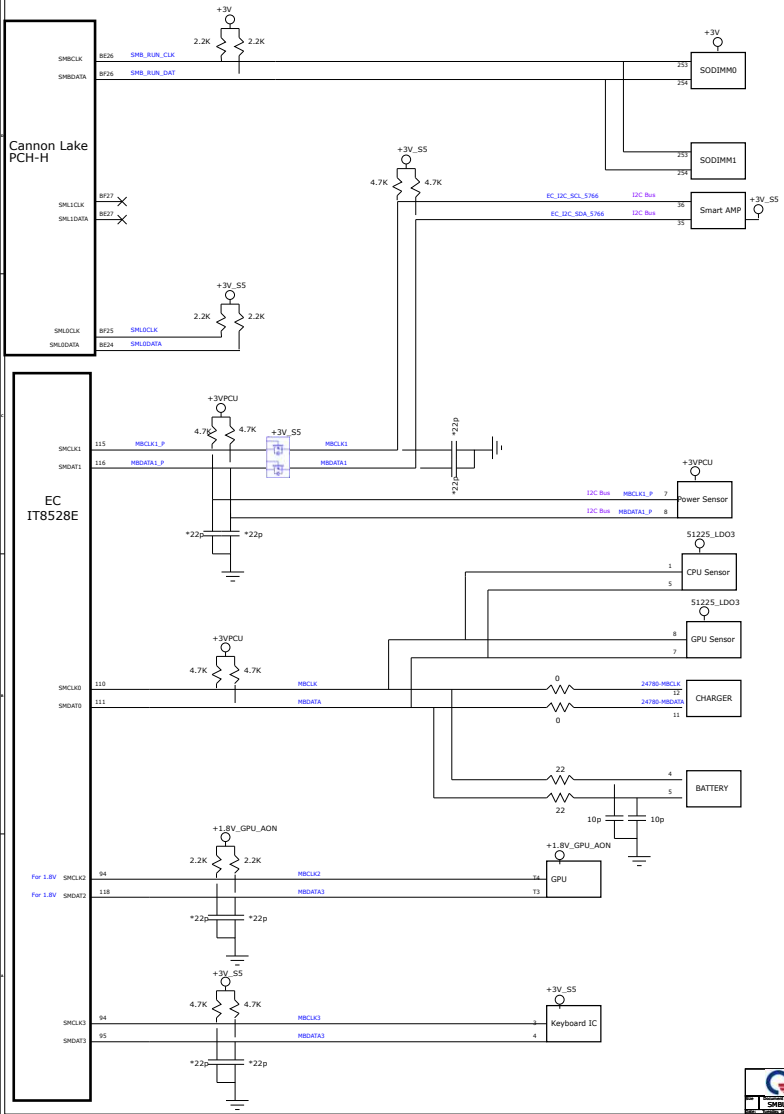
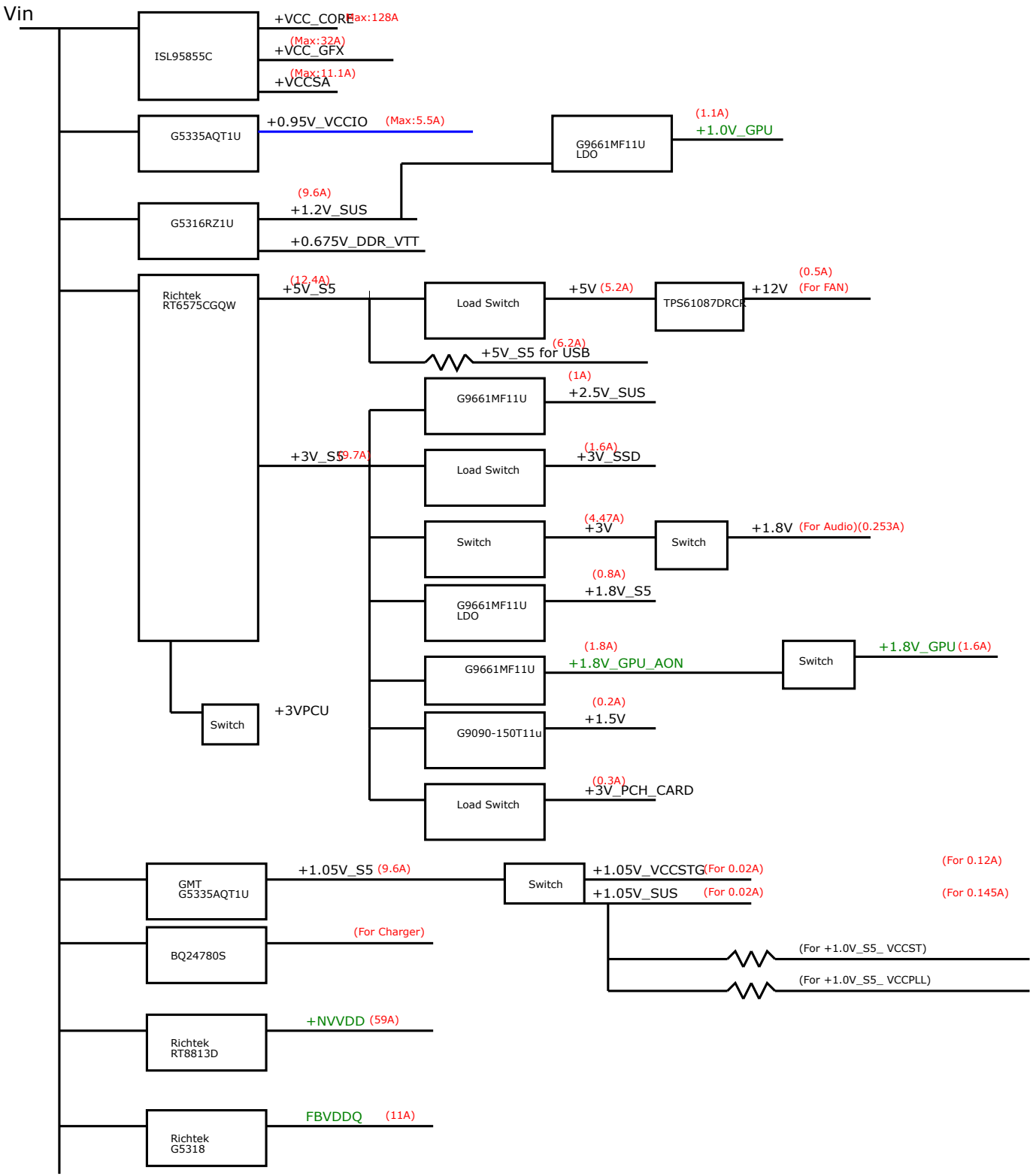

Cannon Lake PCH-H
SMBCLK
SMBDATA
BE26
BF26
SMB_RUN_CLK
SMB_RUN_DAT
+3V
2.2K
2.2K
SODIMM0
SODIMM1
253
254
257
254
+3V_S5
4.7K
4.7K
SML1CLK
SML1DATA
BF27
BE27
EC_I2C_SCL_5766
EC_I2C_SDA_5766
I2C Bus
Smart AMP
36
35
SML0CLK
SML0DATA
BF25
BE24
SML0CLK
SML0DATA
EC IT8528E
+3VPCU
SMCLK1
SMDAT1
115
116
MBCLK1_P
MBDATA1_P
MBCLK1
MBDATA1
*22p
Power Sensor
7
8
51225_LDO3
CPU Sensor
1
5
GPU Sensor
9
7
SMCLK0
SMDAT0
110
111
MBCLK
MBDATA
0
24780-MBCLK
24780-MBDATA
12
11
CHARGER
22
BATTERY
4
5
10p
+1.8V_GPU_AON
For 1.8V
SMCLK2
SMDAT2
94
118
MBCLK2
MBDATA3
GPU
T4
T3
SMCLK3
SMDAT3
95
Keyboard IC
3
4



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PROJECT : BKLB & BKNB

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	Power Diagram	1A
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