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NOTES:

1.HSF Property: Comply iSupplier system HSF property attribute up-to-date value.

STRIX 2021

AMD CEZANNE-H + NV_GN20_E3/E5/E7

2020.09.24

<https://realschematic.com>

DATE	CHANGE NO.	REV
21-OCT-2002		

DESIGN / DRAWER	XXX	DATE	21-OCT-2002
CHECK			
APPROVAL			
FILE NAME	60xxxxxxxxxx	PCB VER	XXX
PCB P/N			

INVENTEC			
TITLE	MODEL, PROJECT, FUNCTION	SIZE	CODE
	MAIN BOARD	A3	CS
	DOC. NUMBER		
	1.3.10xxxxx-0-0		
	SHEET	of	119

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RED:POWER
BLUE:APU
GREEN:GPU

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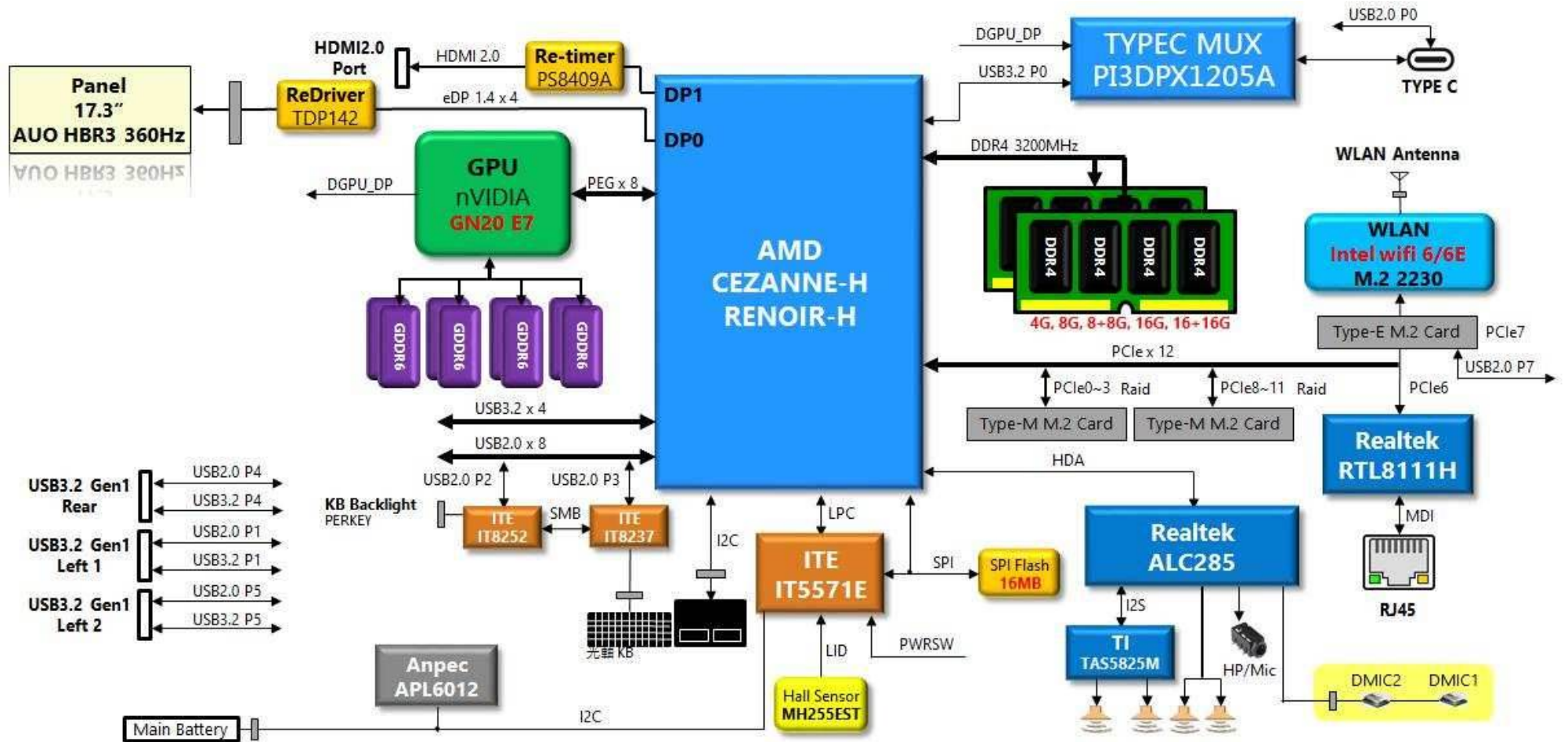
<https://realschematic.com>

INVENTEC

TITLE		MODEL PROJECT FUNCTION	
TABLE OF THE CONTENT		DOC.NUMBER	REV
SIZE	A3	1310xxxxx-0-0	X01
CODE	CS		
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CHANGE BY	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

G533 BLOCK DIAGRAM



BOM SKU CFG

A:AMP
 AC:AMP CODEC
 P:PERKEY
 Z:4ZONE BACKLIGHT
 AP:PERKEY BACKLIGHT
 AZ:NORMAL KEYBOARD
 O:OPTICAL MECHANICAL

V:V-CUT LED
 L:LOGO LED
 N:NFC LED
 K:KEY STONE
 AA:MIC CN FOR 15"
 AB:MIC CN FOR 17"

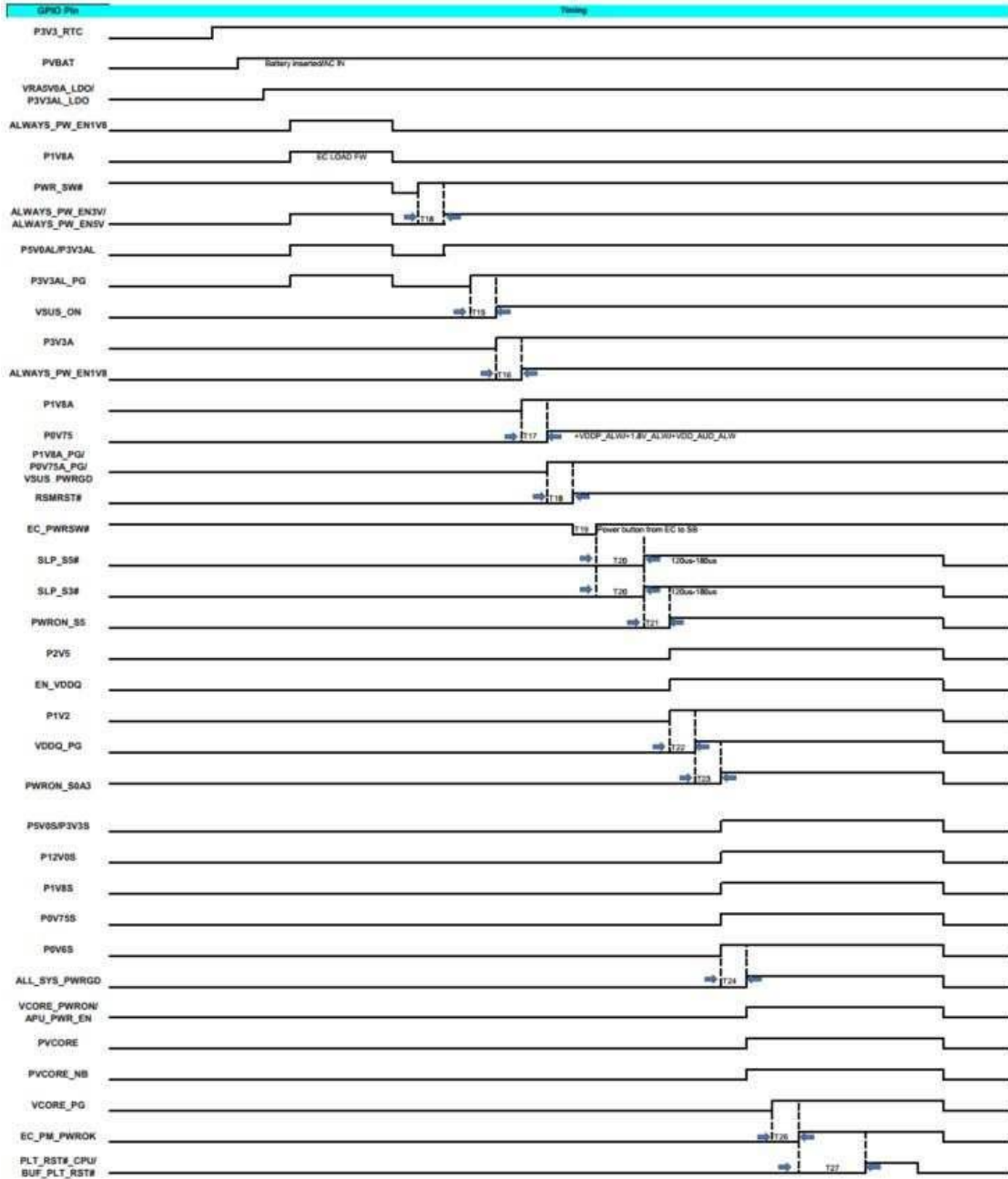
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INVENTEC

TITLE			
MODEL PROJECT,FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

POWER SEQUENCE



SIGNAL	VOTAGE	G3	S5	S3	S0	REMARK
P3V3AL_RTC	3.3V	0	0	0	0	COIN BATTERY
PVBAT	19V	X	0	0	0	DC-IN ALWAYS
P3V3AL	3.3V	X	0	0	0	DC-IN ALWAYS
P5V0AL	5V	X	0	0	0	DC-IN ALWAYS
P3V3A	3.3V	X	0	0	0	
P0V75A	0.75V	X	0	0	0	
P1V8A	1.8V	X	0	0	0	
P2V5	2.5V	X	X	0	0	
P1V2	1.2V	X	X	0	0	
P5V0S	5V	X	X	X	0	
P3V3S	3.3V	X	X	X	0	
P1V8S	1.8V	X	X	X	0	
P0V75S	0.75V	X	X	X	0	
P0V6S	0.6V	X	X	X	0	
PVCORE	SVC/SVD	X	X	X	0	
PVCORE_NB	SVC/SVD	X	X	X	0	

Table 42. Power Sequencing Group Definitions with Coin Cell Battery

Group	System Power Domain	Voltages
Group A	G3	VDDBT_RTC_G
Group B	S5	VDD_33_S5, VDD_18_S5, VDDIO_AUDIO, VDOP_S5,
	S3	VDDIO_MEM_S3
Group C	S0	VDD_33, VDD_18, VDDP; (Add delay (>1ms) between VDD_33 and VDD_18 ramp up power sequence).
Group D	S0	VDDCR_SOC, VDDCR_CPU** (AM4 only), VDDCR* (FP6 only)

INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3 CODE CS 1310xxxx-0-0 REV X01

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CHANGE by: XXX DATE: 21-OCT-2002
PCB P/N: 60xxxxxxxxx PCB VER: XXX

SIZE A3 CODE CS 1310xxxx-0-0 REV X01

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HSIO MAP

AMD Cezanne-H				
Mode		X60/SCAR	X50	AMD CRB
Display	DP0	eDP	eDP	eDP
	DP1	HDMI	HDMI	DP
USB 2.0	Port 0	TypeC	TypeC	TypeC
	Port 1	USB3 TypeA Left1	USB3 TypeA Left1	USB3 TypeA
	Port 2	IT8298	IT8298	USB2 TypeA
	Port 3	IT8237	NC	Camera
	Port 4	USB3 TypeA_REAR	USB3 TypeA_REAR	TypeC
	Port 5	USB3 TypeA Left2	USB3 TypeA Left2	USB3 TypeA
	Port 6	NC	NC	USB2 CN
	Port 7	Bluetooth	Bluetooth	USB2 CN
USB 3.0	Port 0	TypeC	TypeC	TypeC
	Port 1	USB3 TypeA Left1	USB3 TypeA Left1	USB3 TypeA
	Port 4	USB3 TypeA_REAR	USB3 TypeA_REAR	TypeC
	Port 5	USB3 TypeA Left2	USB3 TypeA Left2	USB3 TypeA
PEG X8	Port [0:7]	NV GN20 E3/E4/E5/E7	NV GN20 P0/P1	PCIE SLOT
PCIE	Port 0	PCIE SSD1	PCIE SSD1	SSD1
	Port 1			
	Port 2			
	Port 3			
	Port 4	NC	NC	SLOT
	Port 5	NC	NC	WWAN
	Port 6	Ethernet	Ethernet	Ethernet
	Port 7	WLAN	WLAN	WLAN
	Port 8	PCIE SSD2	PCIE SSD2	SSD2
	Port 9			
Port 10				
Port 11				
GPU	DP	GN20 E3/E4/E5/E7: IFPC	GN20 P0/P1: IFPE	

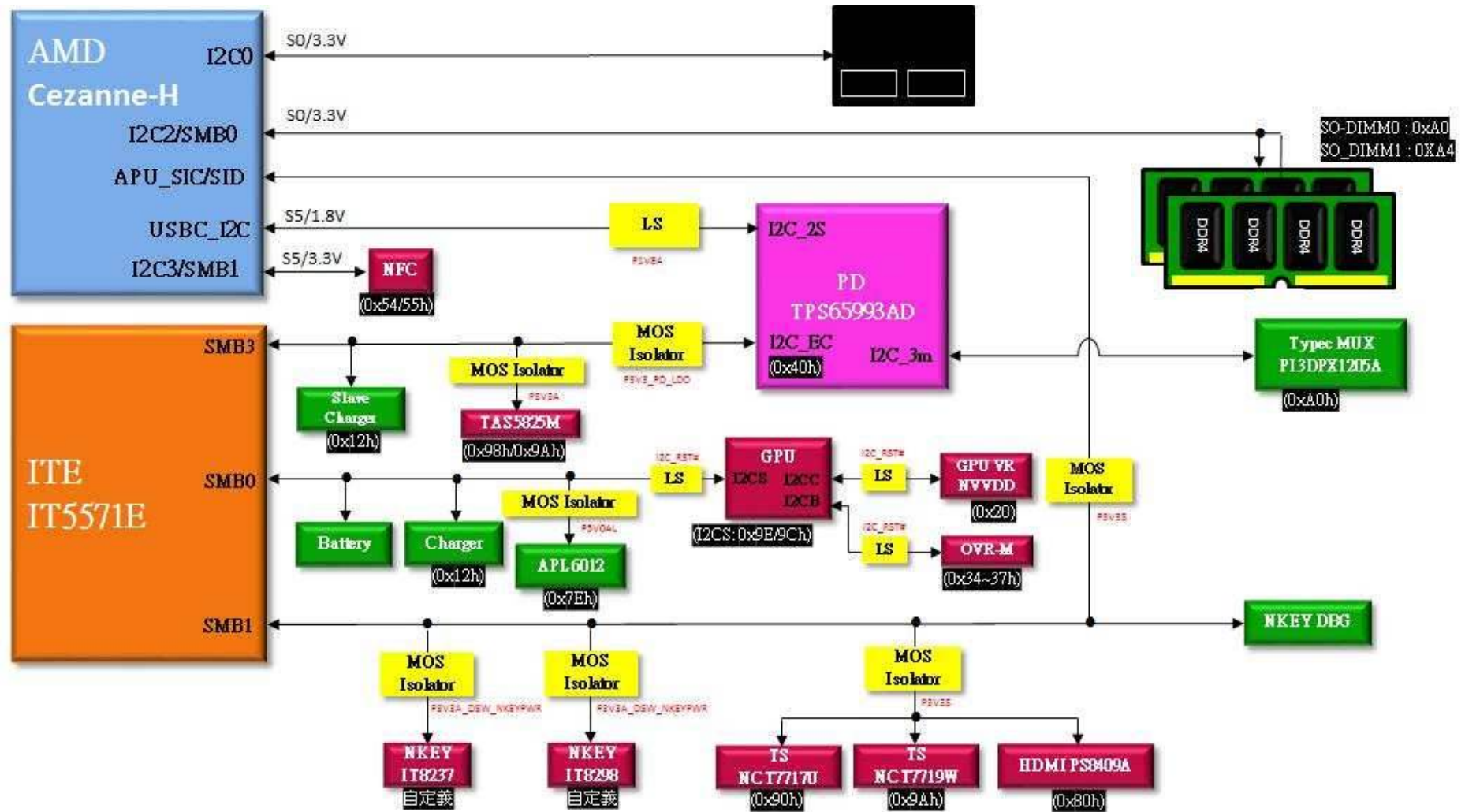
	Normal KB 4Zone+Func Key	Normal KB PerKey RGB+Func Key	Optical KB 4Zone+Func Key	Optical KB PerKey RGB+Func Key
IC	ITE	ITE	ITE	ITE
	IT8298 (ASUS: IT8299)	IT8298 (ASUS: IT8299)	IT8298 (ASUS: IT8299)	IT8298 (ASUS: IT8299)
功能	N-Key+ LED特效控制	N-Key+ LED特效控制	N-Key+ LED特效控制	N-Key+ LED特效控制
IC		ITE	ITE	ITE
		IT8013 (ASUS: IT8013)	IT8237 (ASUS: IT8237)	IT8237 (ASUS: IT8237)
功能	https://realschema.com	LED特效控制	N-KEY+ KB GPIO SCAN	N-KEY+ KB GPIO SCAN

INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC NUMBER	REV X01
		1310xxxx-0-0	
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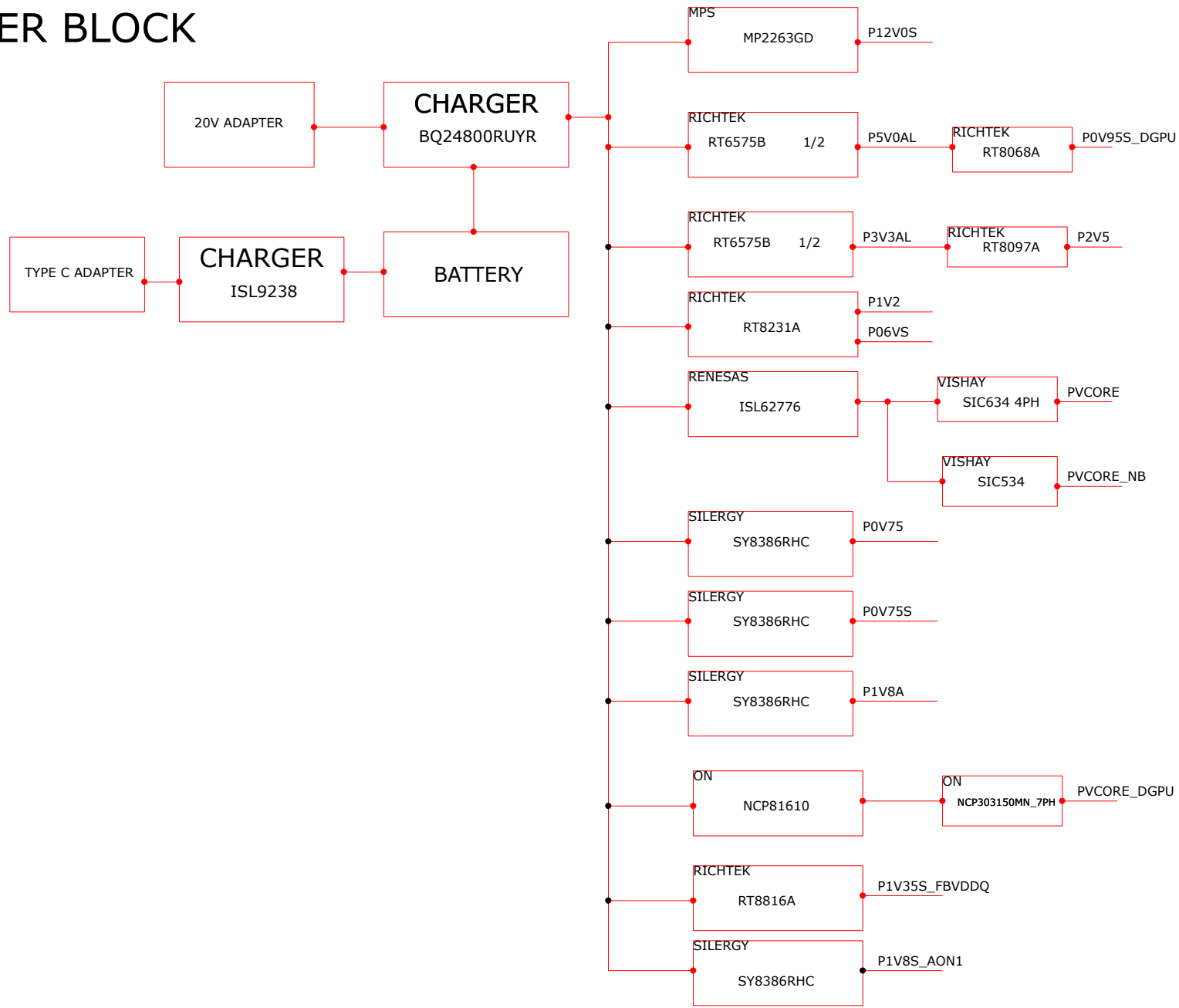
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SMBUS DIAGRAM



INVENTEC					
TITLE					
MODEL, PROJECT, FUNCTION					
Block Diagram					
SIZE	CODE	DOC NUMBER	REV		
A3	CS	1310xxxx-0-0	X01		
CHANGE by	DATE	21-OCT-2002			
PCB P/N	PCB VER	XXX			
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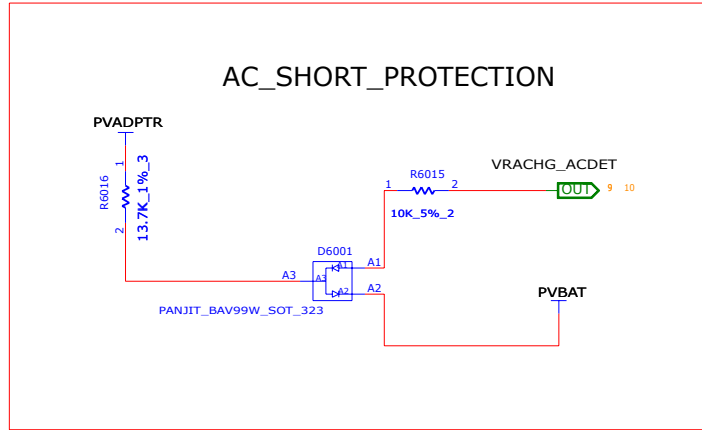
POWER BLOCK



INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by	DATE	DATE	DATE
PCB P/N	60xxxxxxxxxx	21-OCT-2002	XXX
PCB VER.	XXX		
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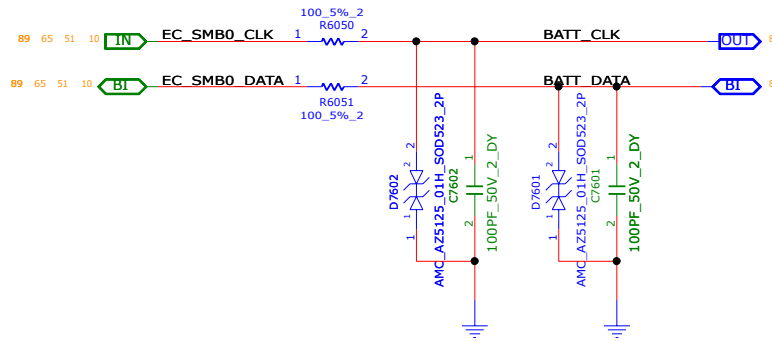
BATTERY / AC SHORT PROTECTION

LOCATION NUMBER : 6000~6999



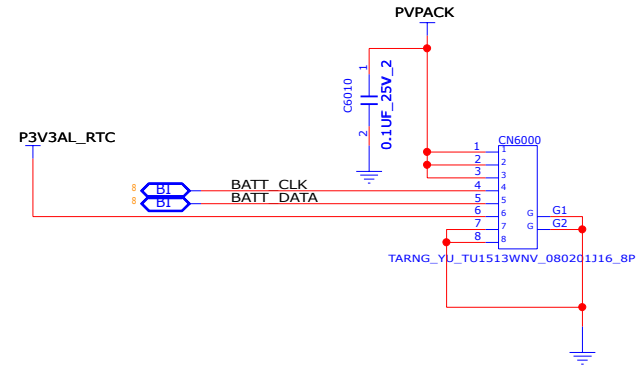
BATTERY PIN DEFINE

BATTERY SIDE		MAIN BOARD SIDE	
PIN1	P+	PIN1	P+
PIN2	P+	PIN2	P+
PIN3	SMBC	PIN3	P+
PIN4	SMBD	PIN4	SMBC
PIN5	RTC	PIN5	SMBD
PIN6	P-	PIN6	RTC
PIN7	P-	PIN7	P-
		PIN8	P-



BATT

I2C ADDR W/R 0XFE/0XFF



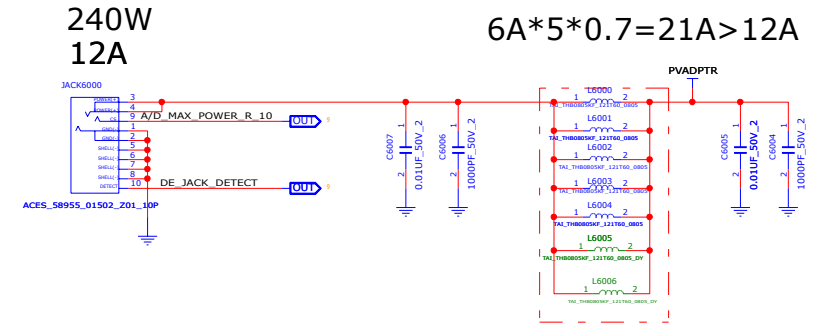
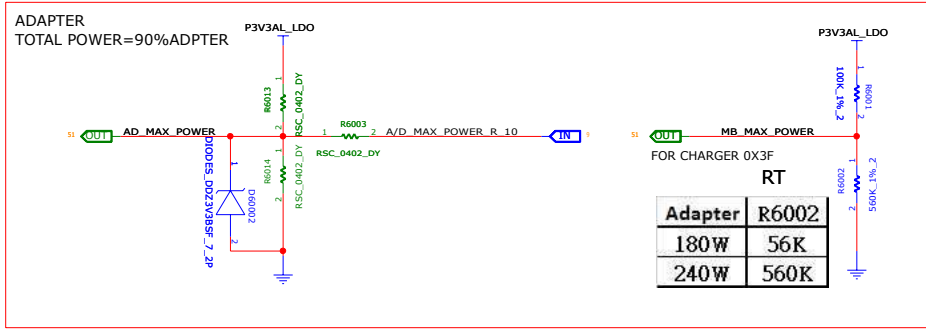
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INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by	DATE	21-OCT-2002	
PCB P/N	PCB VER.	XXX	
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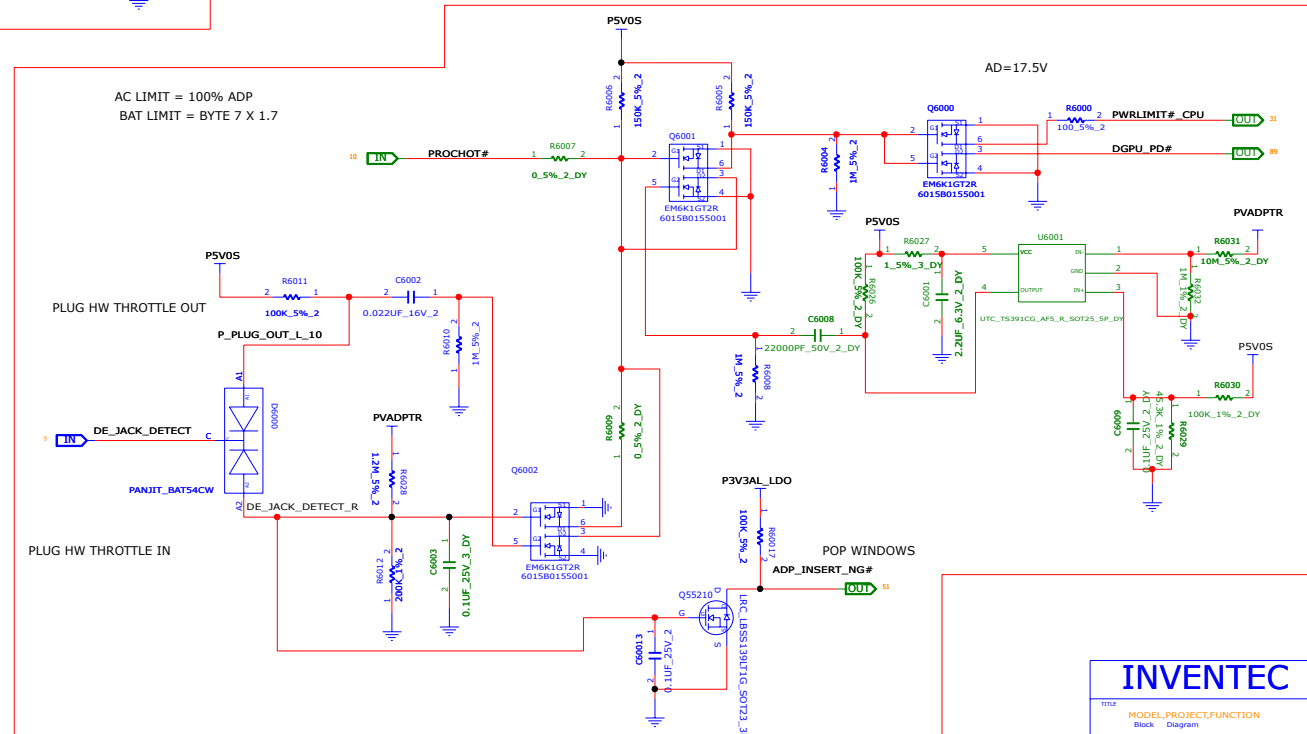
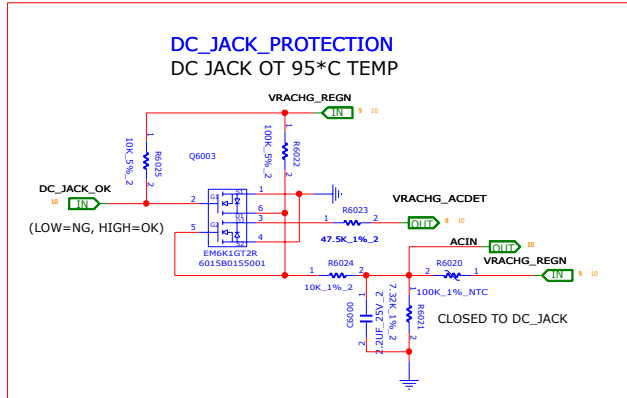
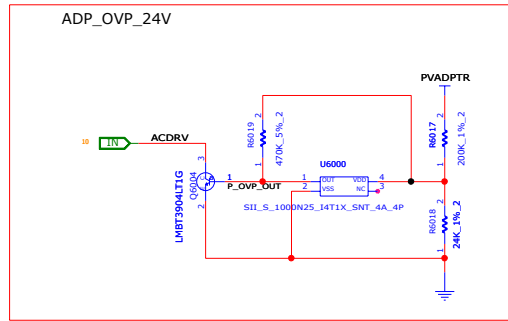
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PCB P/N	60xxxxxxxxxx	PCB VER.	XXX
SIZE	A3	CODE	CS
		DOC. NUMBER	1310xxxxx-0-0
		REV	X01
		SHEET	8 of 119

DC_IN

LOCATION NUMBER : 6000~6999



RT	N_SERIES		G_SERIES	
	10MOHM	5MOHM		
14K	0.4V	45W	120W	
31.6K	0.8V	150W	150W	
56K	1.2V	180W	180W	
93.1K	1.6V	65W	230W	
150K	2V	N/A	280W	
270K	2.4V	90W	200W	
560K	2.8V	120W	240W	



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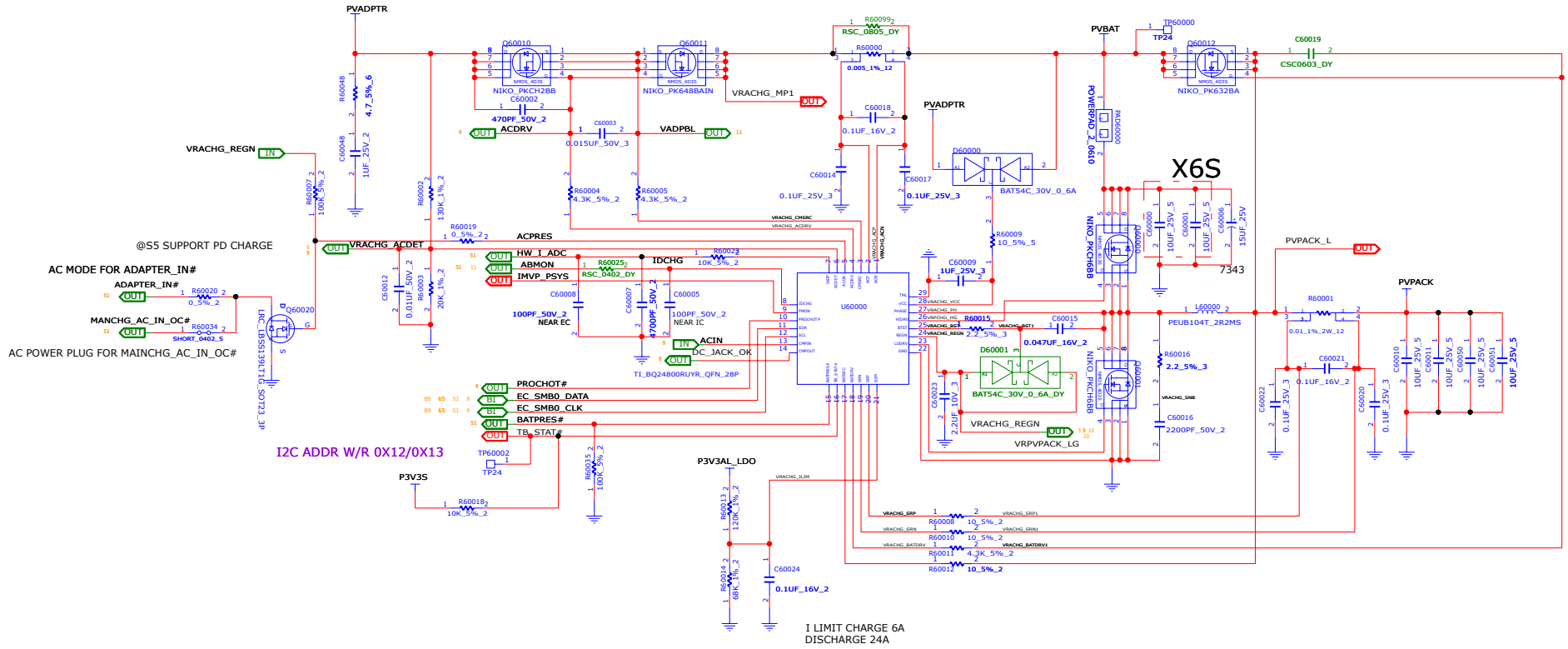
INVENTEC

TITLE	Block	Diagram
MODEL_PROJECT_FUNCTION		
SIZE	CODE	SPIC NUMBER
A1	CS	1310xxxx-B-B
REV	X01	

CHANGE BY	XXX	DATE	21-OCT-2002
P/CB P/N	6Pxxxxxxx	P/CB VER	XXX
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CHARGER (BQ24800)

LOCATION NUMBER : 60000~60099



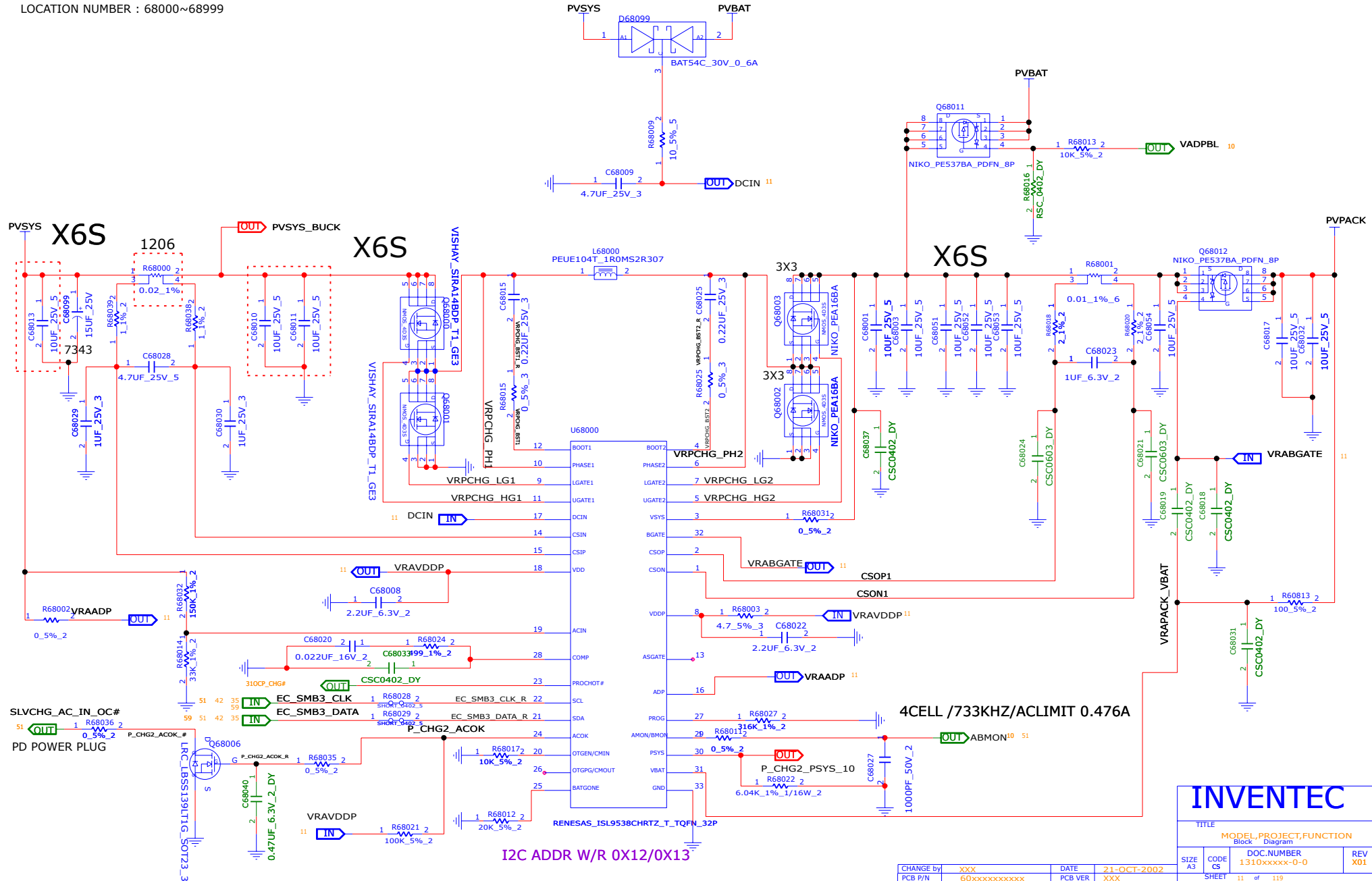
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INVENTEC	
TITLE	MODEL_PROJECT_FUNCTION
Block	Diagram
SIZE	DOC NUMBER
A1	1310xxxxx-0-0
SHEET	REV
11	X01

CHANGE BY	XXX	DATE	21-OCT-2002
PCH P/N	6Pxxxxxxxxxx	PCH VER	XXX

PD IN CHARGER (ISL9538C)

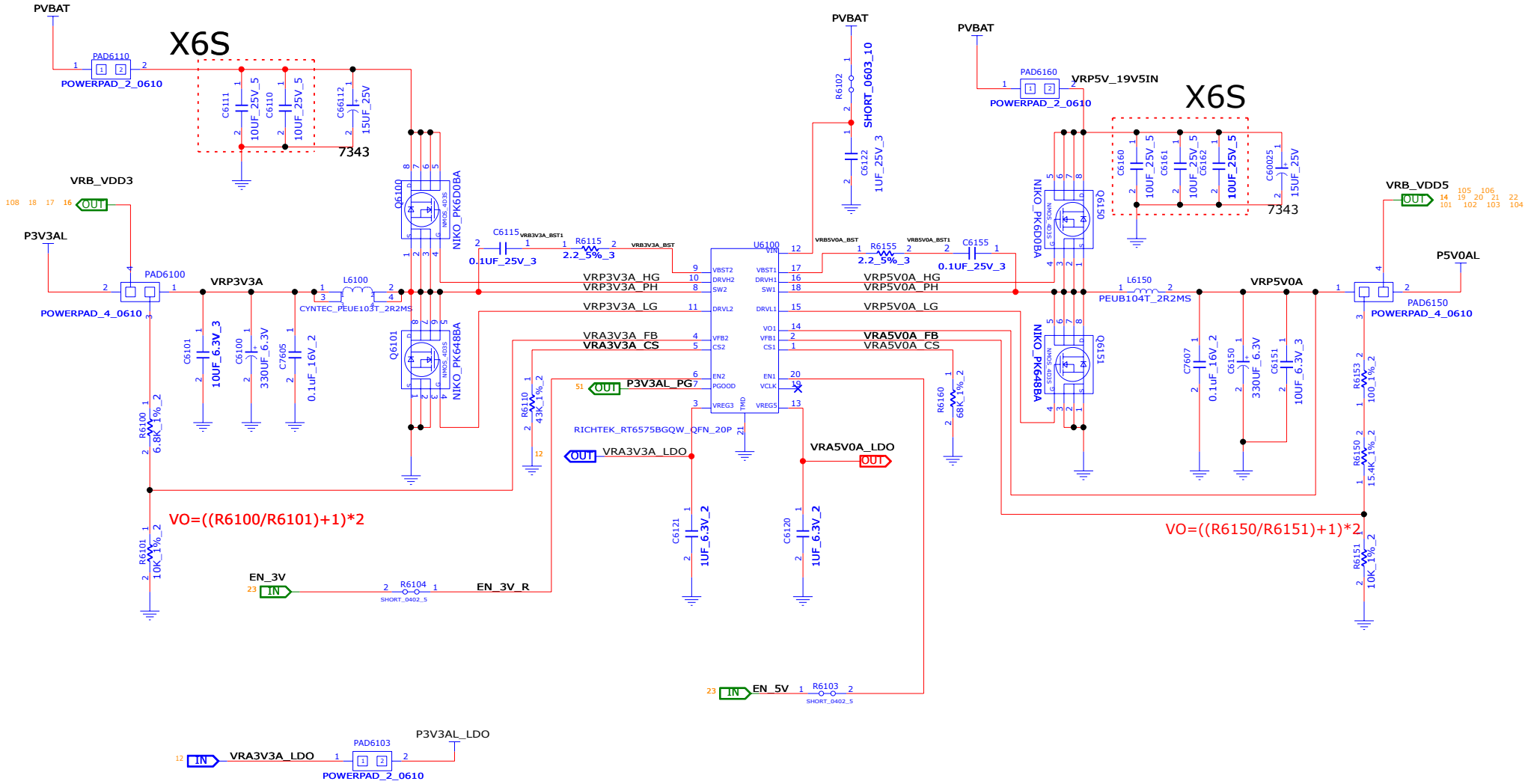
LOCATION NUMBER : 68000~68999



INVENTEC			
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MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by		DATE	
PCB P/N		PCB VER	
XXX		21-OCT-2002	XXX
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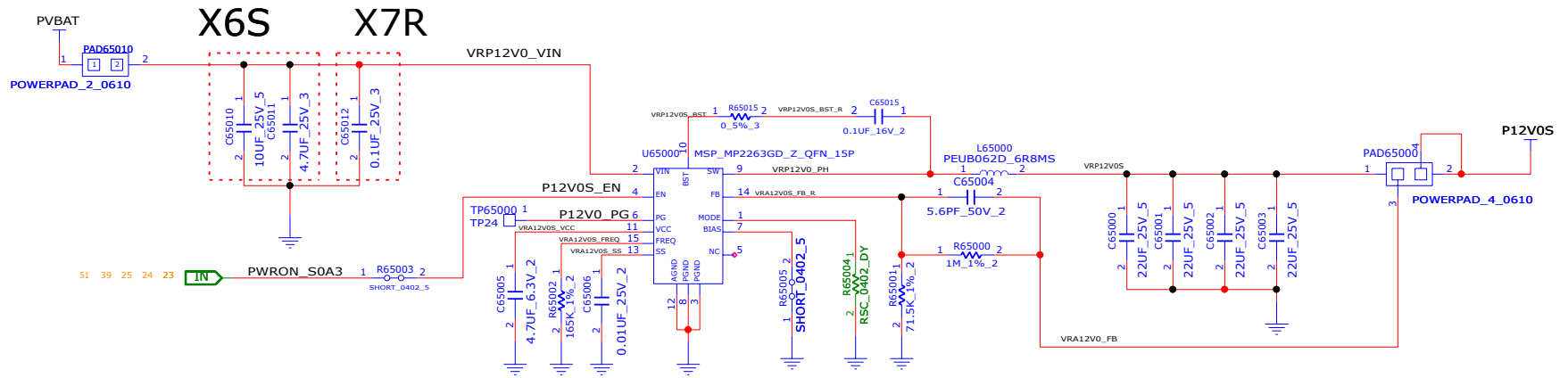
P3V3AL / P5V0AL (RT6575B)

LOCATION NUMBER : 6100~6199



P12V0S (MP2263GD)

LOCATION NUMBER : 65000~65999



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INVENTEC			
TITLE MODEL_PROJECT,FUNCTION PVCCG1			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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PCB P/N	60xxxxxxxxxx	PCB VER	XXX
SIZE	A3	CODE	CS
DOC.NUMBER	1310xxxx-0-0	REV	X01
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P1V2_P0V6S (RT8231A)

LOCATION NUMBER : 60300~60399

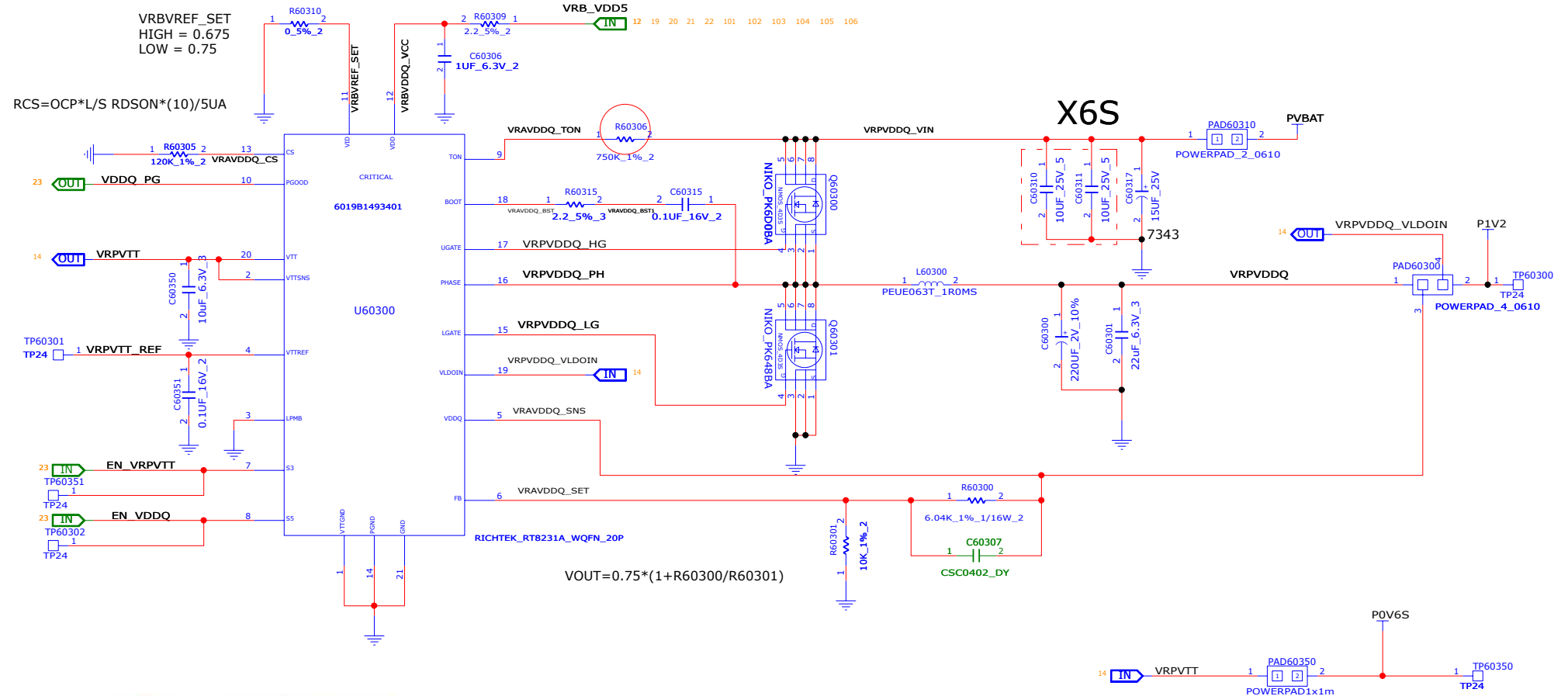


Table 2. S3 and S5 Truth Table

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

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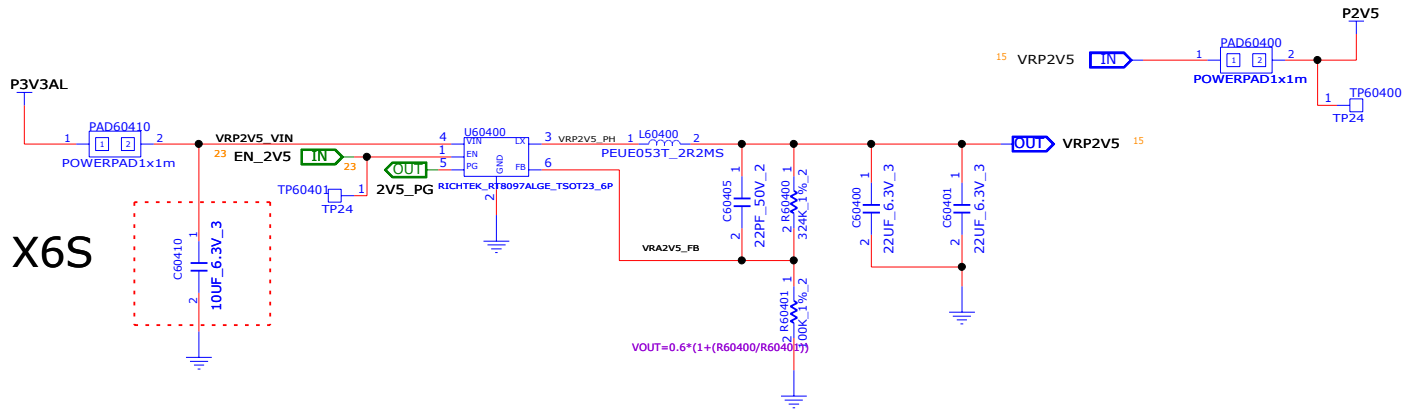
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TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01
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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

P2V5 (RT8097A)

LOCATION NUMBER : 60400~60499



INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
P2V5

SIZE CODE
A3 CS

DOC. NUMBER
1310xxxx-0-0

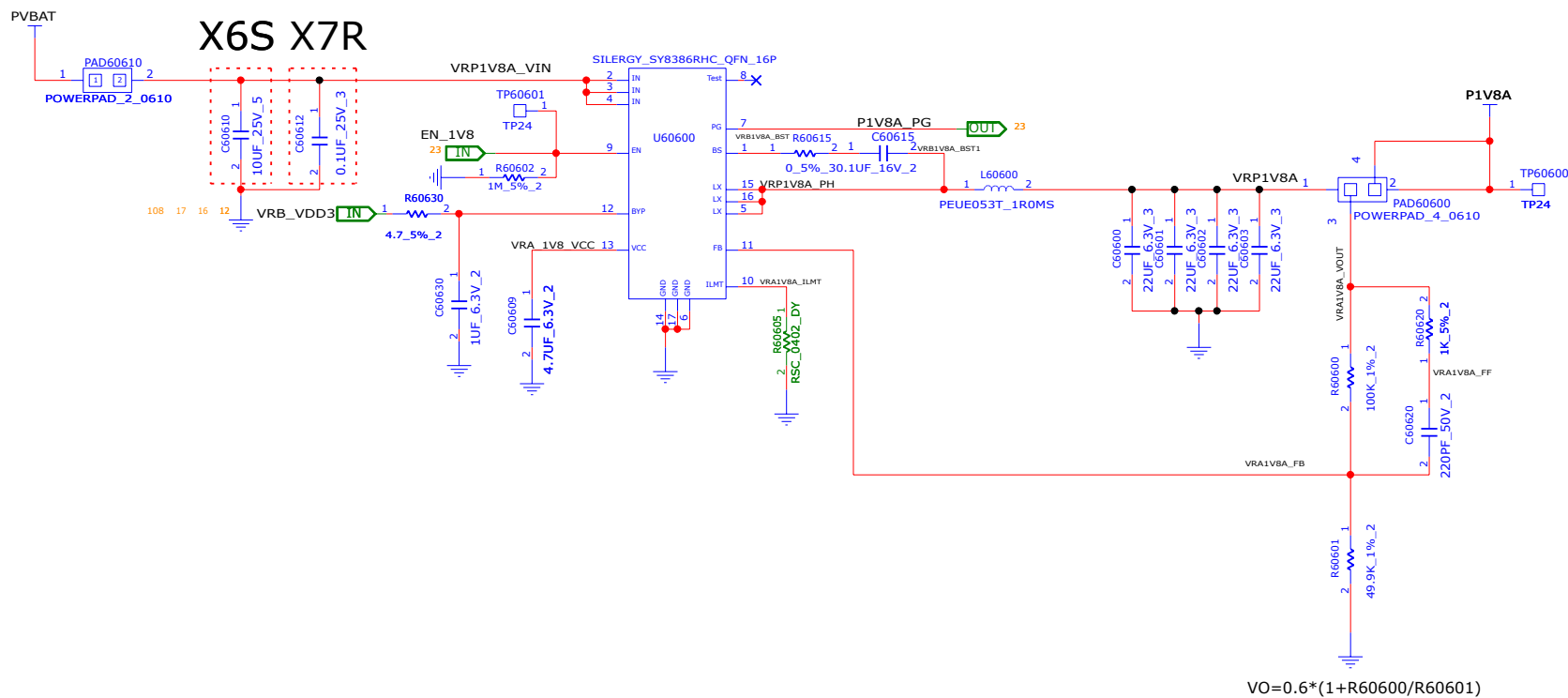
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REV
X01

CHANGE by: XXX DATE: 21-OCT-2002
PCB P/N: 60xxxxxxxxx PCB VER: XXX

P1V8A (SY8386R)

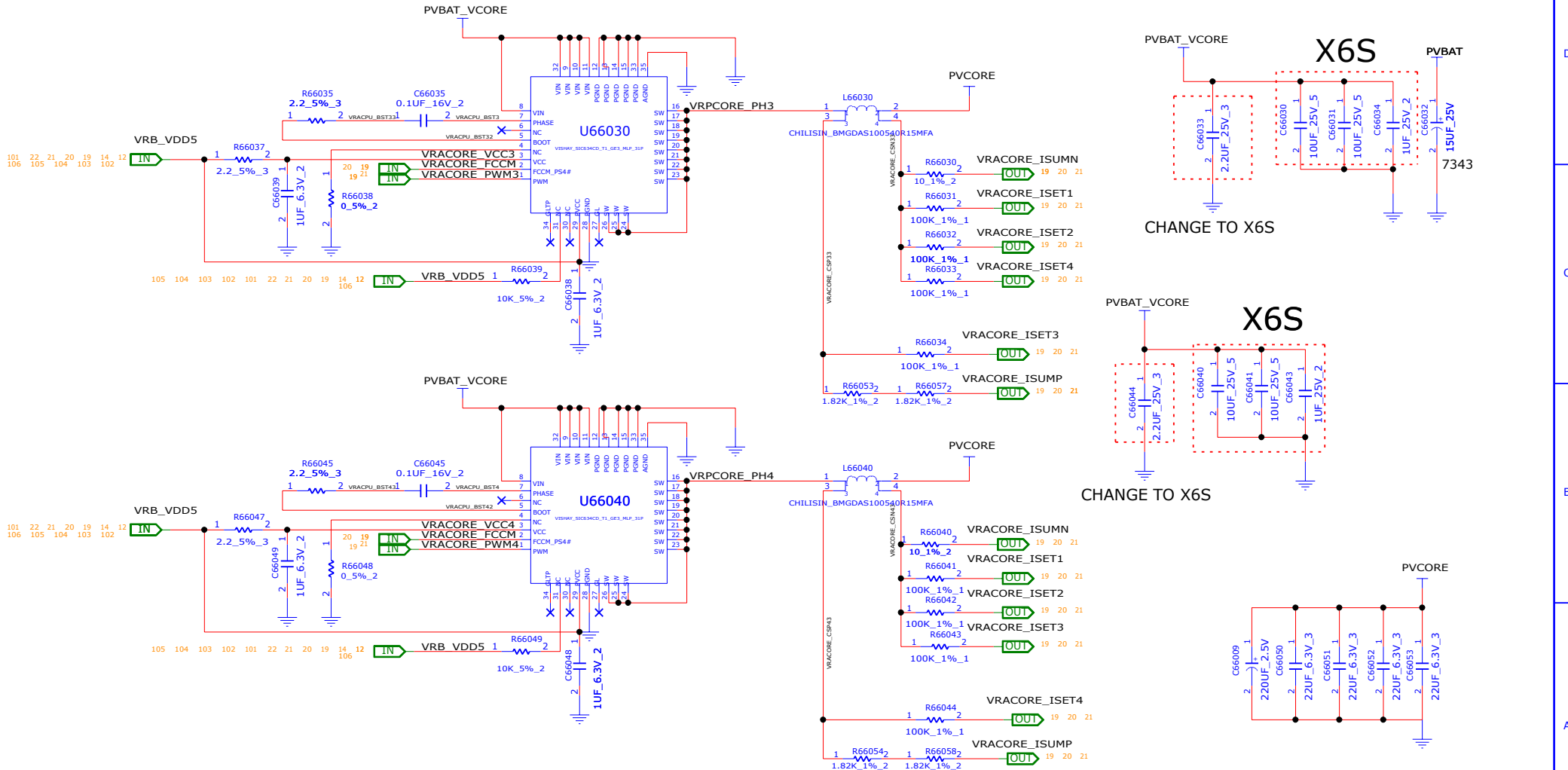
LOCATION NUMBER : 60600~60699



INVENTEC			
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MODEL, PROJECT, FUNCTION			
Block Diagram			
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A3	CS	1310xxxx-0-0	X01
CHANGE by		DATE	
PCB P/N		PCB VER	
XXX		21-OCT-2002	
60xxxxxxxxxx		XXX	
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PVCORE SIC634_3-4P

LOCATION NUMBER : 66000~66999



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INVENTEC

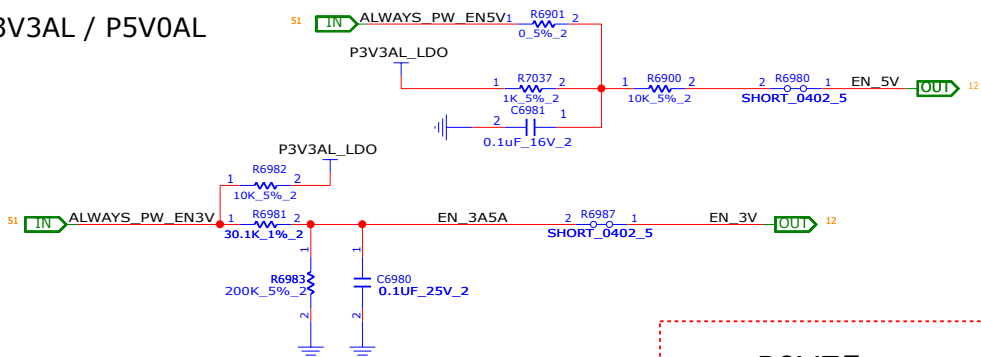
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Block Diagram			
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CHANGE by	XXX	DATE	21-OCT-2002
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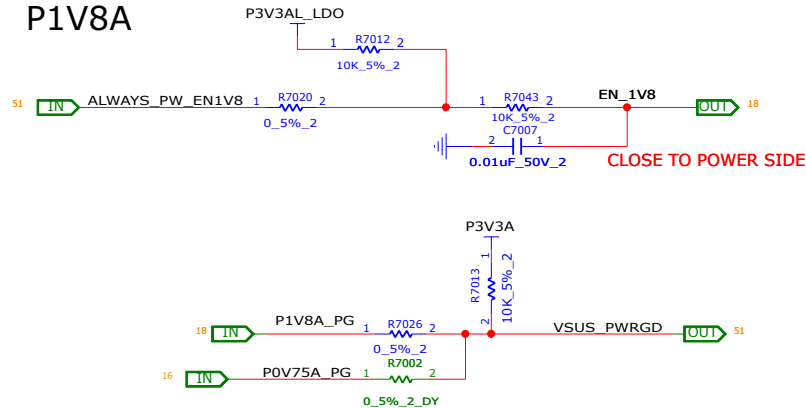
POWER SEQUENCE (1/3)

LOCATION NUMBER : 6900~7099

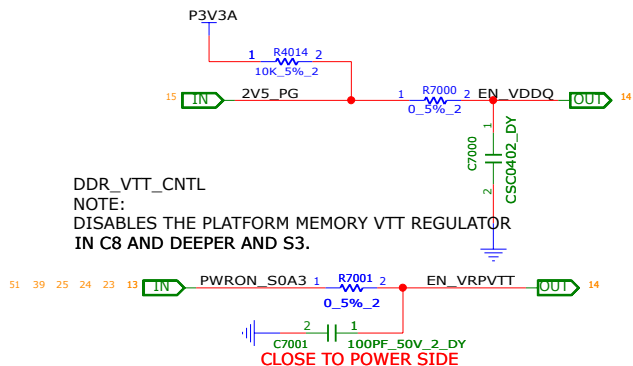
P3V3AL / P5V0AL



P1V8A

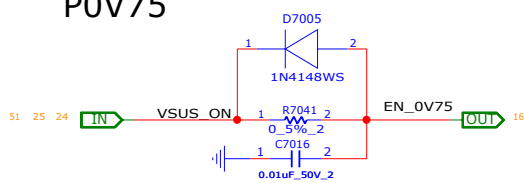


DDR4 P1V2/VTT/VPP

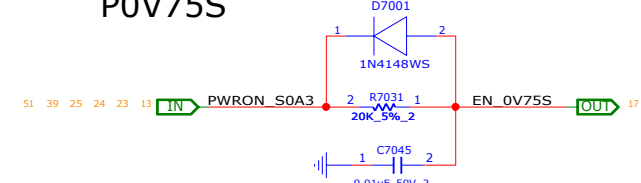


DDR_VTT_CNTL
NOTE:
DISABLES THE PLATFORM MEMORY VTT REGULATOR
IN C8 AND DEEPER AND S3.

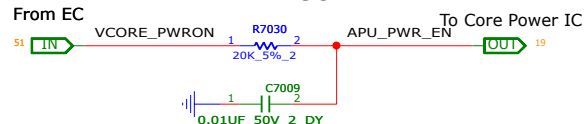
P0V75



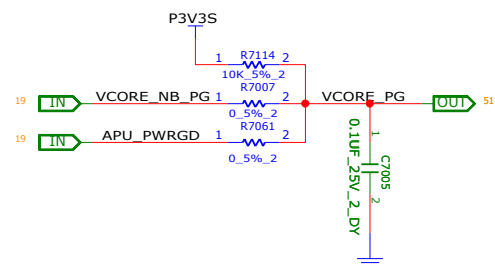
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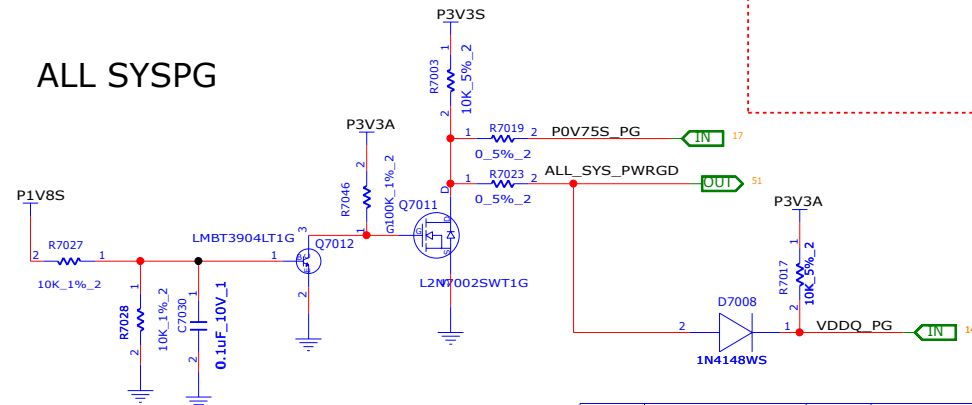
ENABLE PVCORE



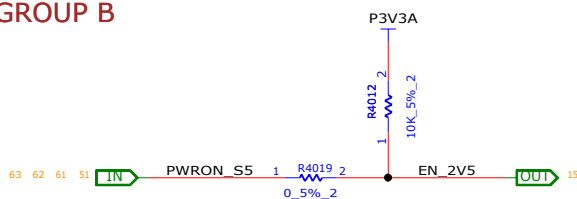
CPU VCORE PWRGD



ALL SYSPG



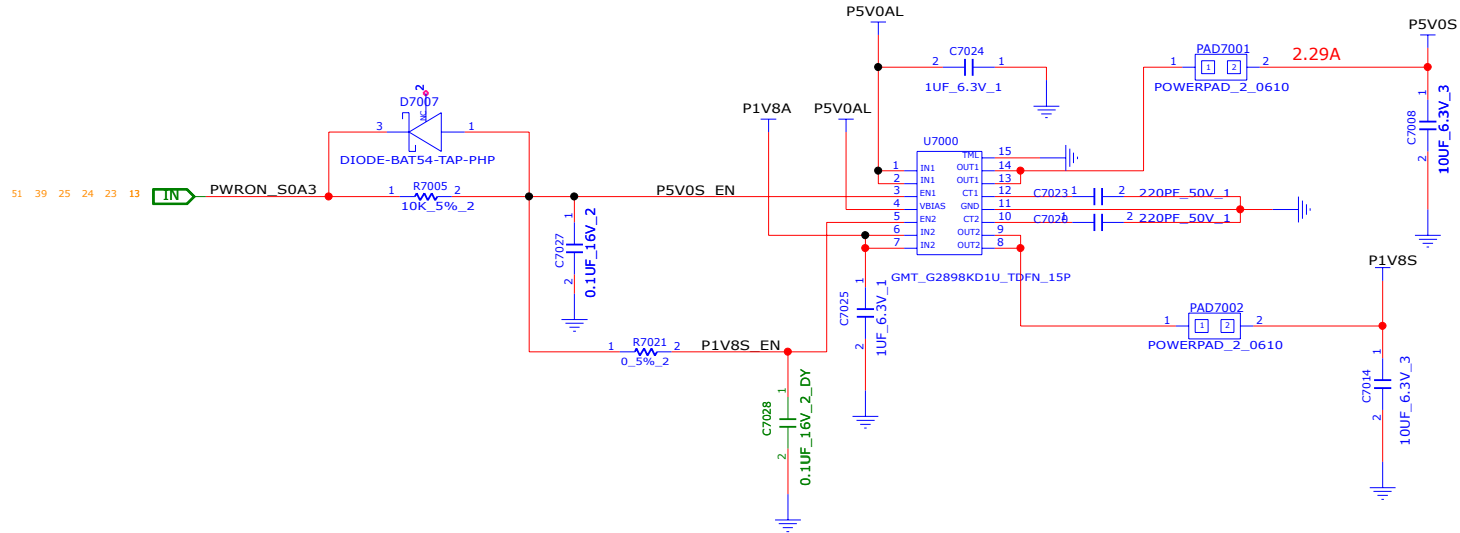
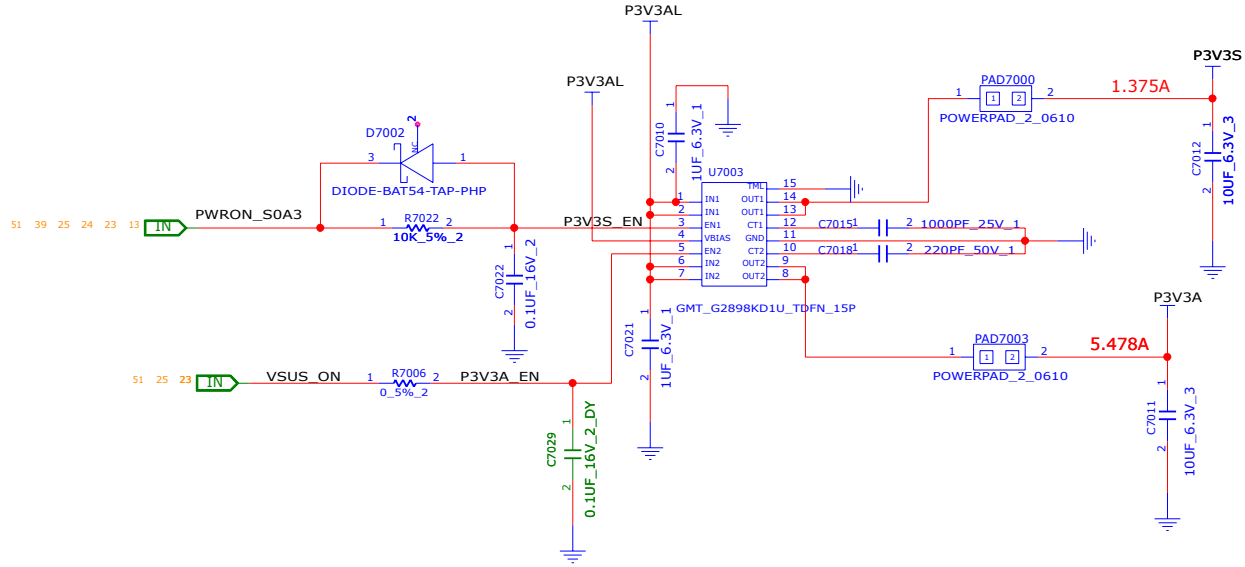
GROUP B



INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by	DATE	21-OCT-2002	
PCB P/N	PCB VER	XXX	
SHEET		23 of 119	

POWER SEQUENCE (2/3)

LOCATION NUMBER : 7000~7099

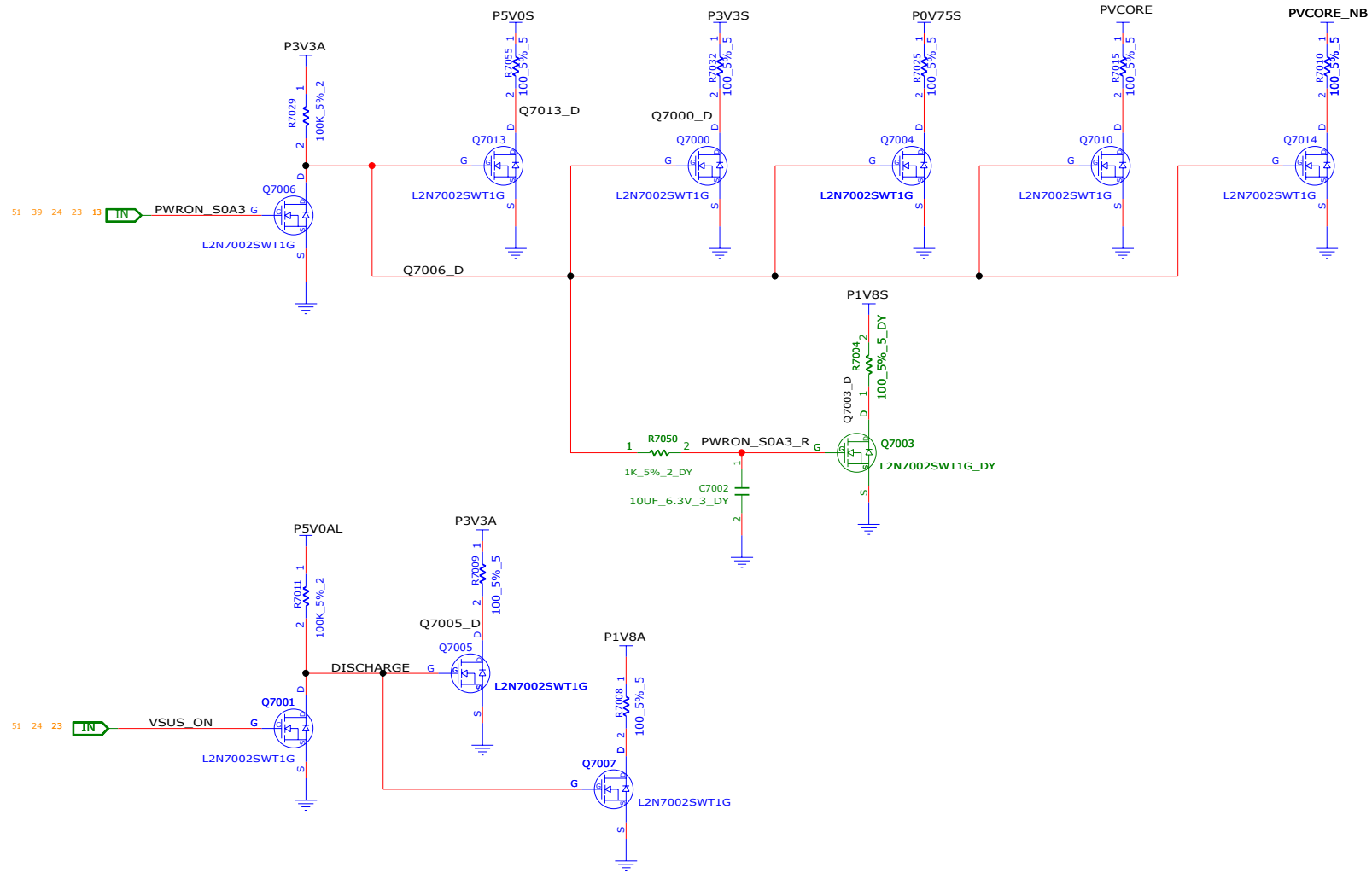


<https://realschematic.com>

INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by		DATE	REV
XXX		21-OCT-2002	XXX
PCB P/N		PCB VER	SHEET
60xxxxxxxxxxx		XXX	24 of 119

POWER SEQUENCE (3/3)

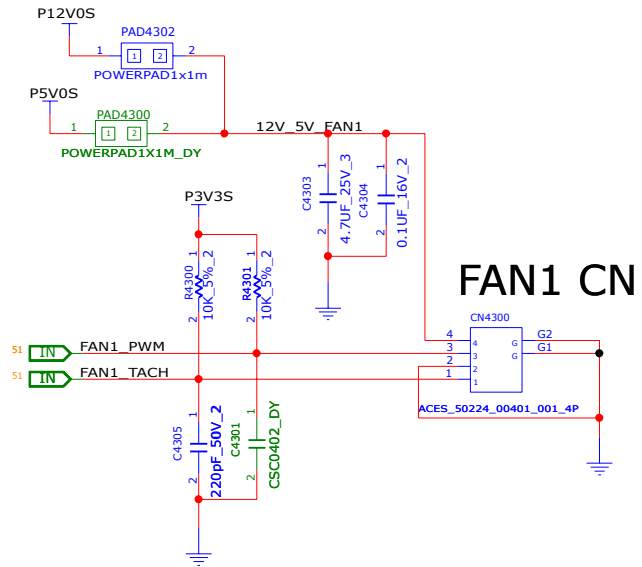
LOCATION NUMBER : 7000~7099



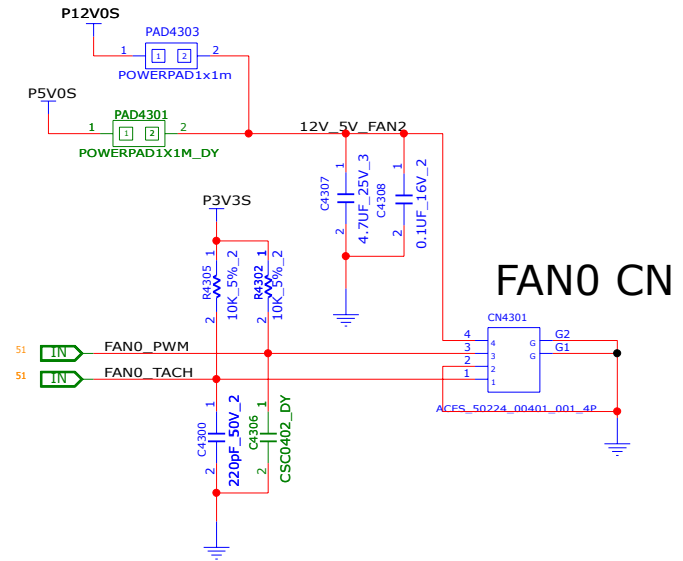
FAN / HALL SENSOR

LOCATION NUMBER : 4300~4349(FAN)
 LOCATION NUMBER : 9100~9199(HALL SENSOR)

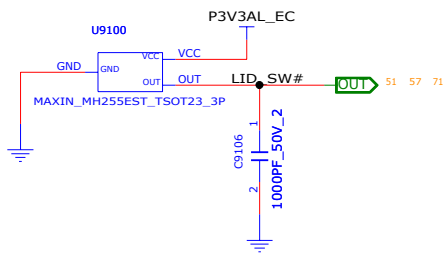
DEFAULT:12V



DEFAULT:12V



HALL_SENSOR



INVENTEC

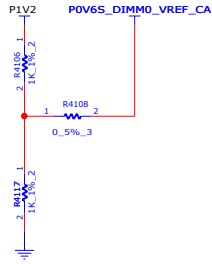
TITLE		MODEL PROJECT FUNCTION	
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 26 of 119			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

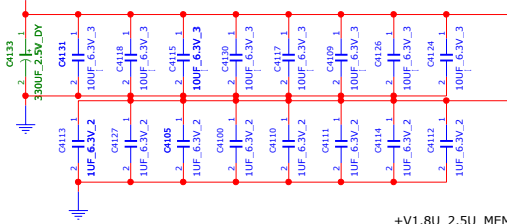
DDR4_DIMM0_CONN

LOCATION NUMBER : 4100~4199(DDR)

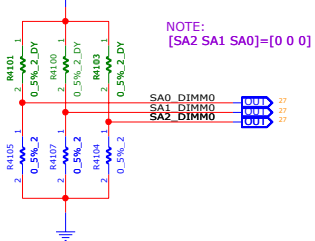
CHA H=4.0MM



+VDD2_MEM P1V2 PLACE THE DISCRETES CLOSE TO SODIMM AND DISTRIBUTE EVENLY ON EACH SIDE OF THE DIMM

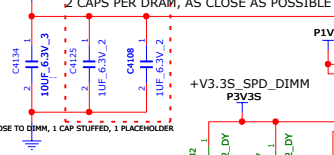


+V3.3S_SPD_DIMM P3V3S



NOTE: [SA2 SA1 SA0]=[0 0 0]

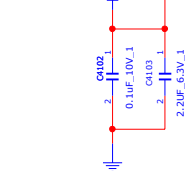
+V_VDD2_VTT POV6S



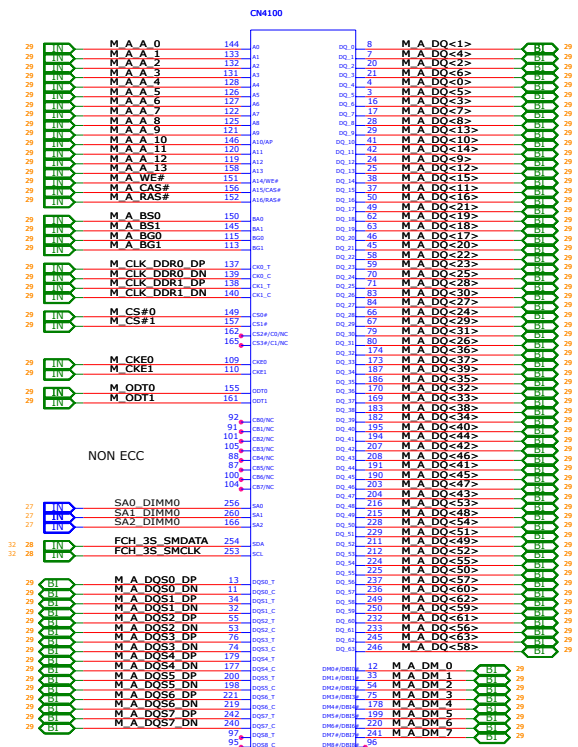
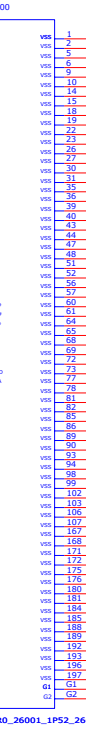
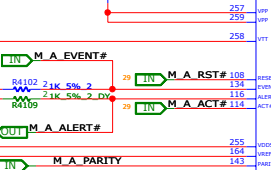
+V3.3S_SPD_DIMM P3V3S



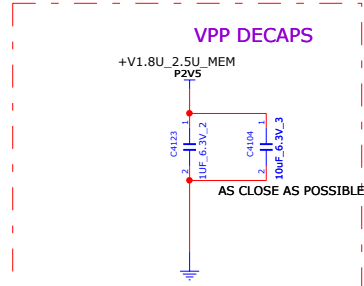
+VREF_CH0_CA POV6S_DIMMO_VREF_CA



+V1.8U_2.5U_MEM P2V5



X50:6026B0328101
X60:6026B0456501



REFERENCE NUMBER: 4100~4199

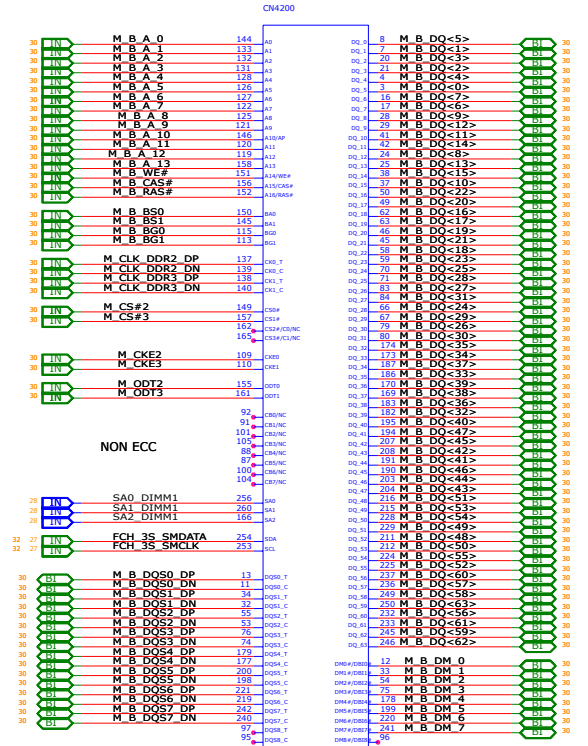
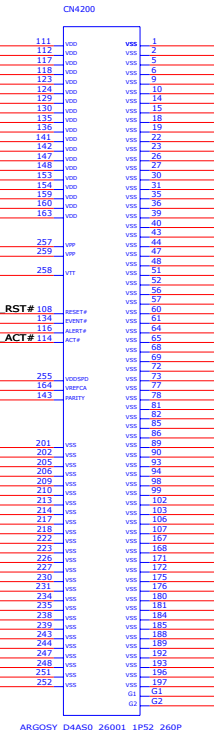
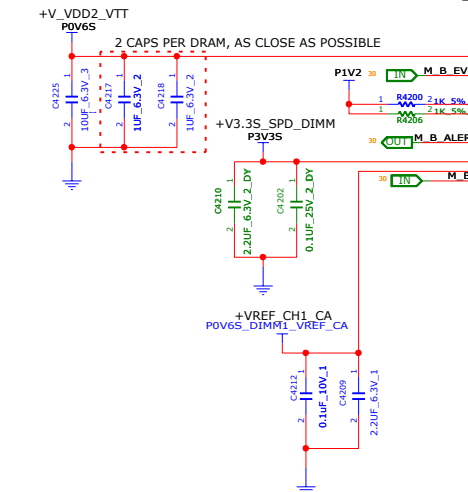
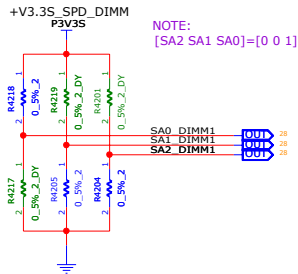
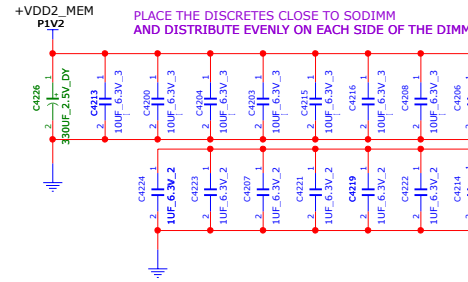
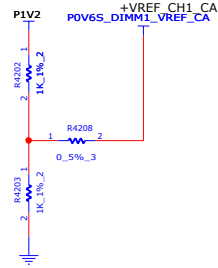
INVENTEC

CHANGE IN	XXX	DATE	21-OCT-2002	DOC NUMBER	REV
PCB P/N	6PXXXXXXXXXX	PCB VER	XXX	1310XXXXX-B-B	X01
SIZE	A1	CODE	CS	37	110
SHEET					

DDR4_DIMM1_CONN

LOCATION NUMBER : 4200~4299(DDR)

CHB H=5.2MM



<https://realschematic.com>
REFERENCE NUMBER:4200~4299

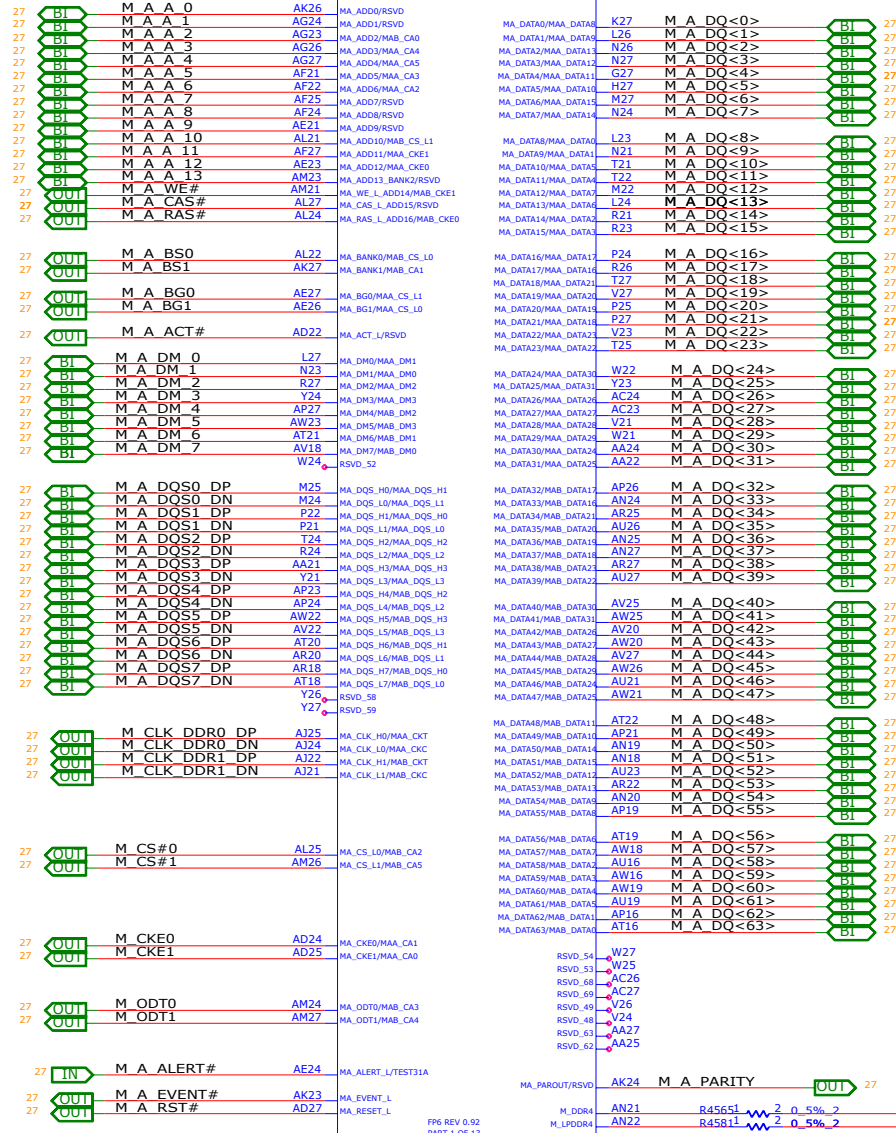
INVENTEC			
TITLE	MODEL_PROJECT/FUNCTION		
Block	Diagram		
SIZE A1	CODE CS	DOC NUMBER 13104xxxx-B-B	REV X01
CHANGE I4	XXX	DATE 21-OCT-2002	
Pcb P/N	6Pxxxxxxx	Pcb VER	XXX
SHEET	38	of	110

APU_FP6_MEMORY CHA

LOCATION NUMBER : 4500~4999(APU)

U4555

MEMORY A



FP6 REV 0.92
PART 1 OF 13

AMD_CEZANNE_H_R7_BGA_FP6_1140P

<https://realschematic.com>

INVENTEC

TITLE: MOD. PROJECT, FUNCTION

DOC. NUMBER: 1310xxxxx-0-0

REV: X01

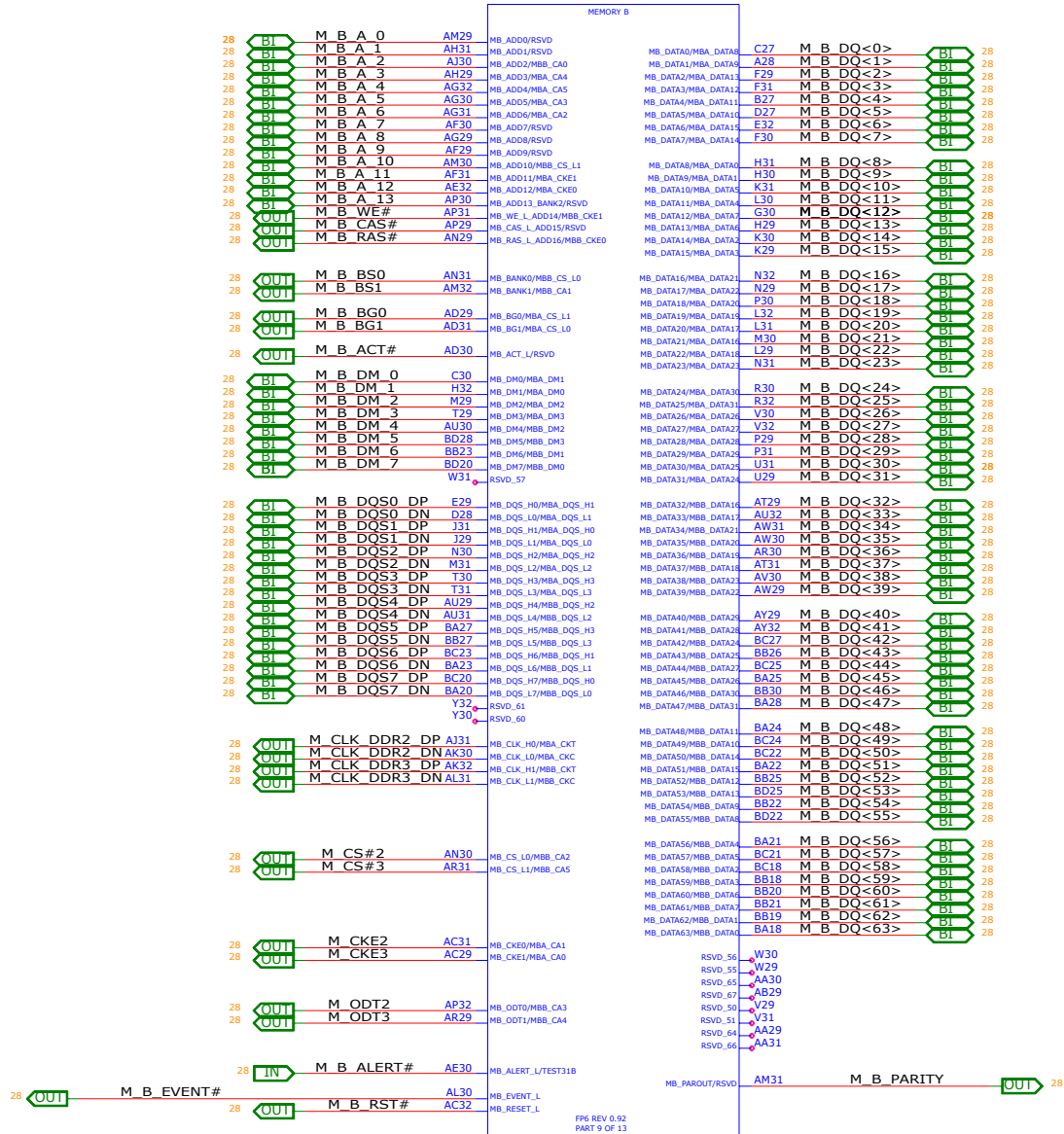
CHANGE by: XXX DATE: 21-OCT-2002
PCB P/N: 60xxxxxxxxxxx PCB VER: XXX

SIZE A3 CODE CS SHEET 29 of 119

APU_FP6_MEMORY_CHB

LOCATION NUMBER : 4500~4999(APU)

U4555



FR6 REV 0.92
PART 8 OF 13

AMD_CEZANNE_H_R7_BGA_FP6_1140P

INVENTEC

TITLE
MCP2598 MODEL S PROPOSED SYSTEM SEQUENCE

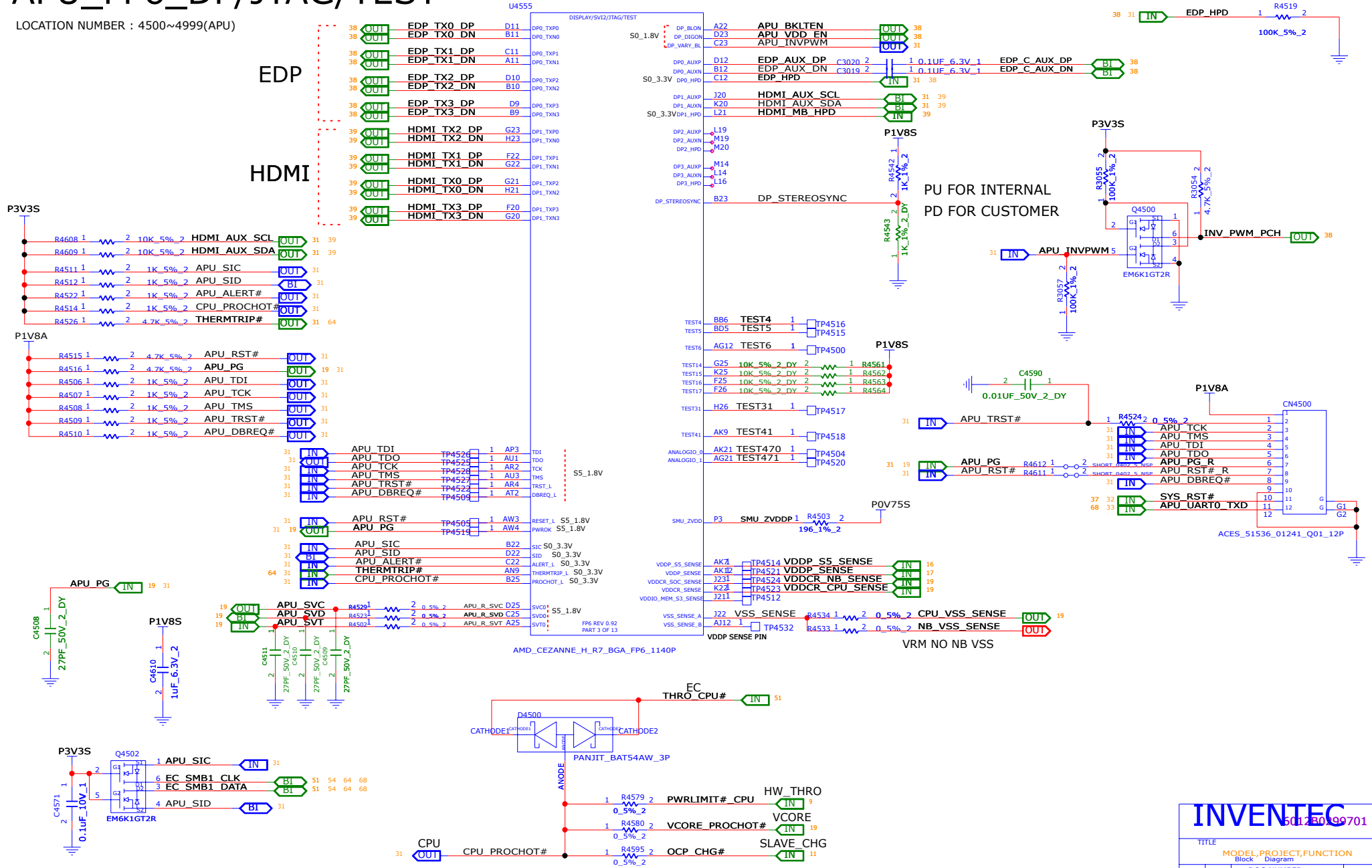
SIZE CODE DOC.NUMBER REV
A3 CS 1310xxxxx-0-0 X01

SHEET 30 of 119

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxxx PCB VER XXX

APU_FP6_DP/JTAG/TEST

LOCATION NUMBER : 4500~4999(APU)



INVENTEC
501230199701

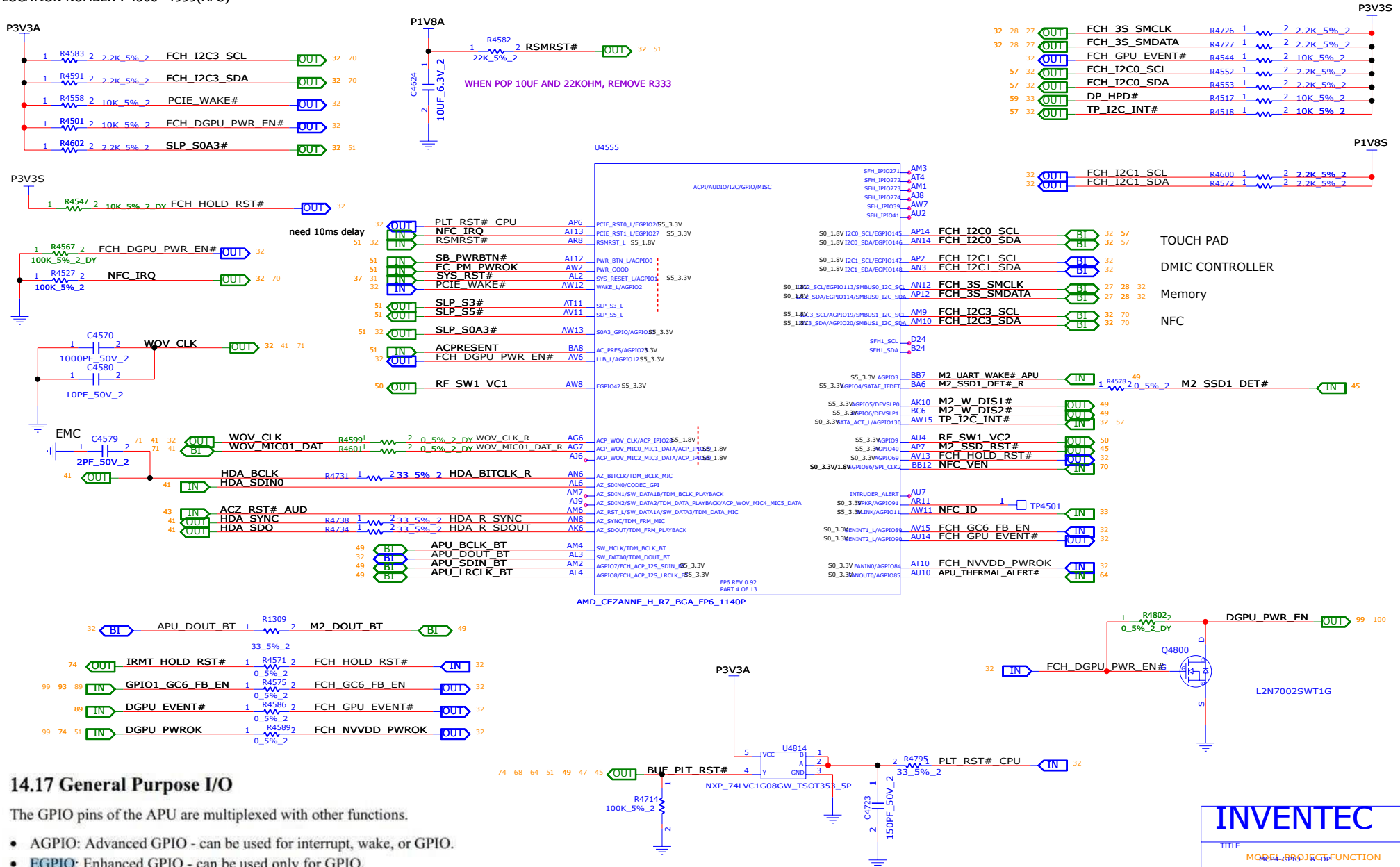
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC. NUMBER 1310XXXX-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	
PCB P/N 60XXXXXXXXXX		PCB VER XXX	
SHEET 31 of 119			

<https://realschematic.com>

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60XXXXXXXXXX	PCB VER	XXX
SIZE	A3	CODE	CS
SHEET	31 of 119	DOC. NUMBER	1310XXXX-0-0
		REV	X01

APU_FP6_I2C_AUDIO

LOCATION NUMBER : 4500~4999(APU)



14.17 General Purpose I/O

The GPIO pins of the APU are multiplexed with other functions.

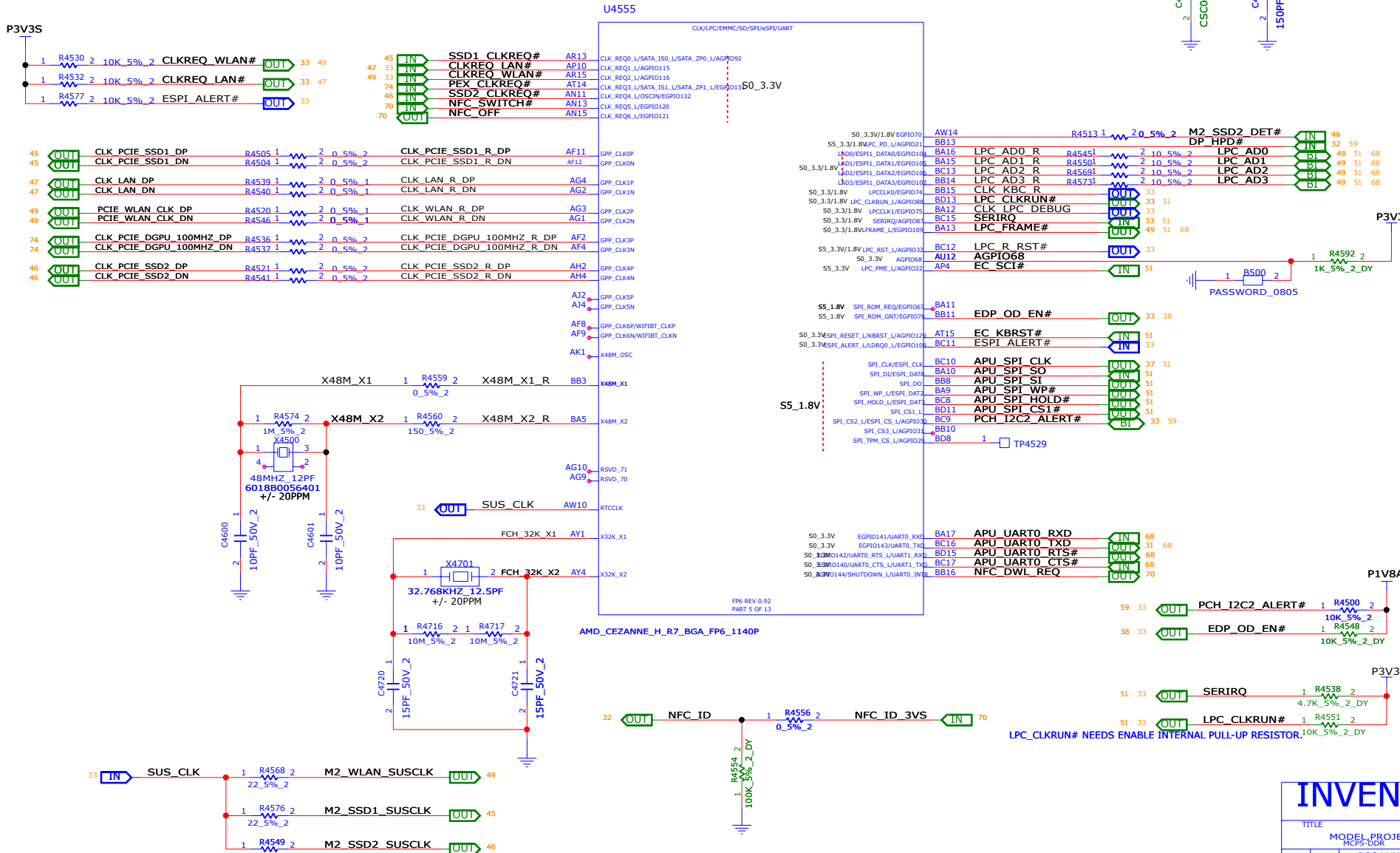
- **AGPIO:** Advanced GPIO - can be used for interrupt, wake, or GPIO.
- **EGPIO:** Enhanced GPIO - can be used only for GPIO.

<https://realschematic.com>

INVENTEC			
TITLE			
MCP41-6P0 PROJECT FUNCTION			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310XXXXX-0-0	X01
CHANGE by		DATE	21-OCT-2002
PCB P/N		PCB VER	XXX
SHEET		32 of 119	

APU_FP6_LPC/SPI/XTAL/GPPCLK

LOCATION NUMBER : 4500~4999(APU)



<https://realschematic.com>

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	XXX

INVENTEC			
TITLE MODEL_PROJECT_FUNCTION MCPS-UBR			
SIZE A3	CODE CS 1	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET	33	of 119	

APU_FP6_PCIE/SATA

LOCATION NUMBER : 4500~4999(APU)

U4555

PCIE



FP6 REV 0.92
PART 2 OF 13

AMD_CEZANNE_H_R7_BGA_FP6_1140P

INVENTEC

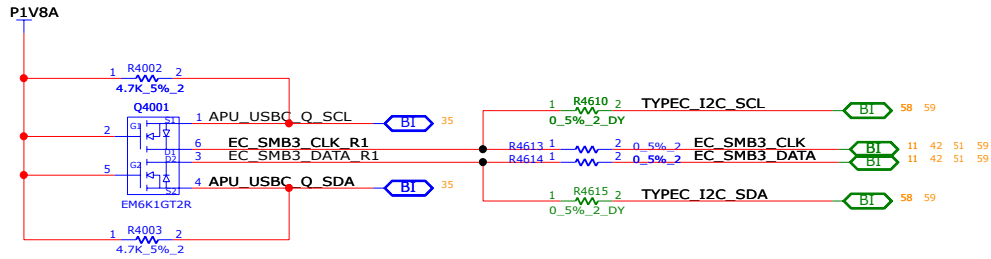
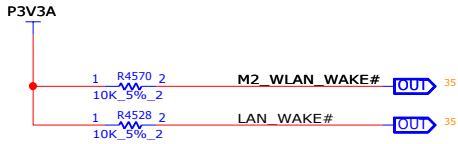
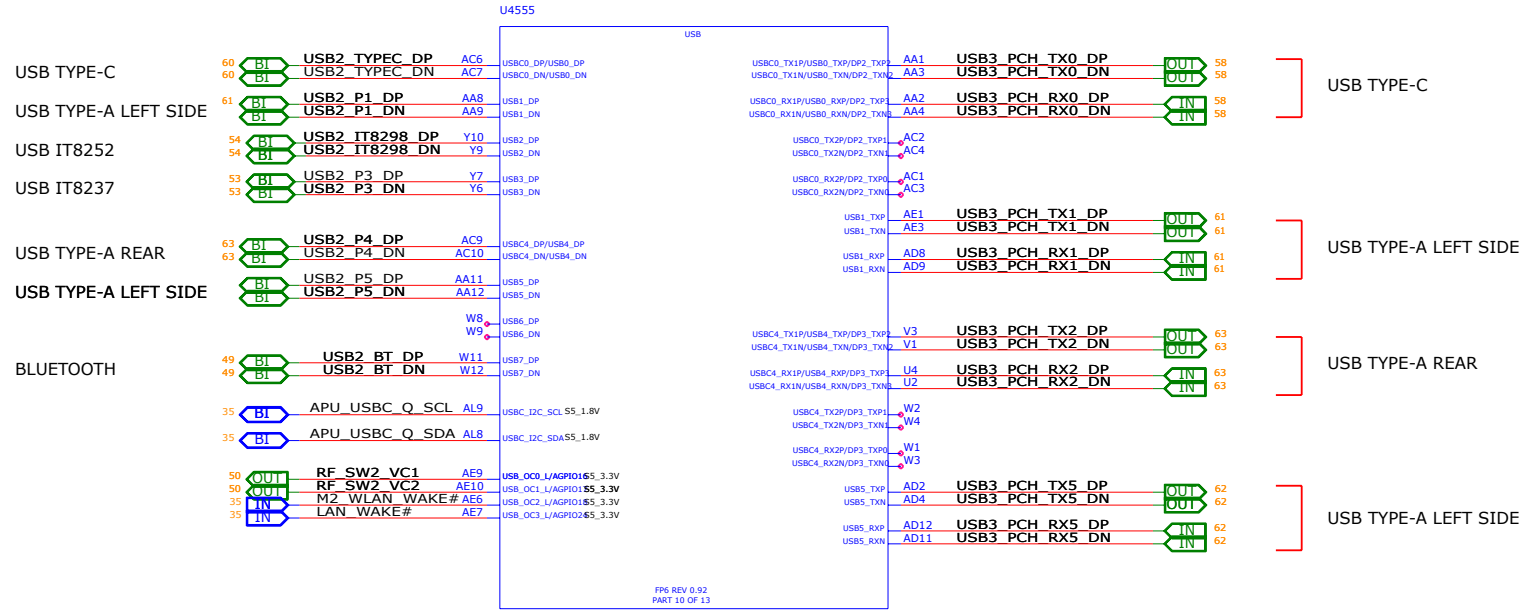
TITLE: MOPRO POWER CONTROL FUNCTION

SIZE A3 CODE CS 1310xxxx-0-0 REV X01
SHEET 34 of 119

CHANGE by: XXX DATE: 21-OCT-2002
PCB P/N: 60xxxxxxxxx PCB VER: XXX

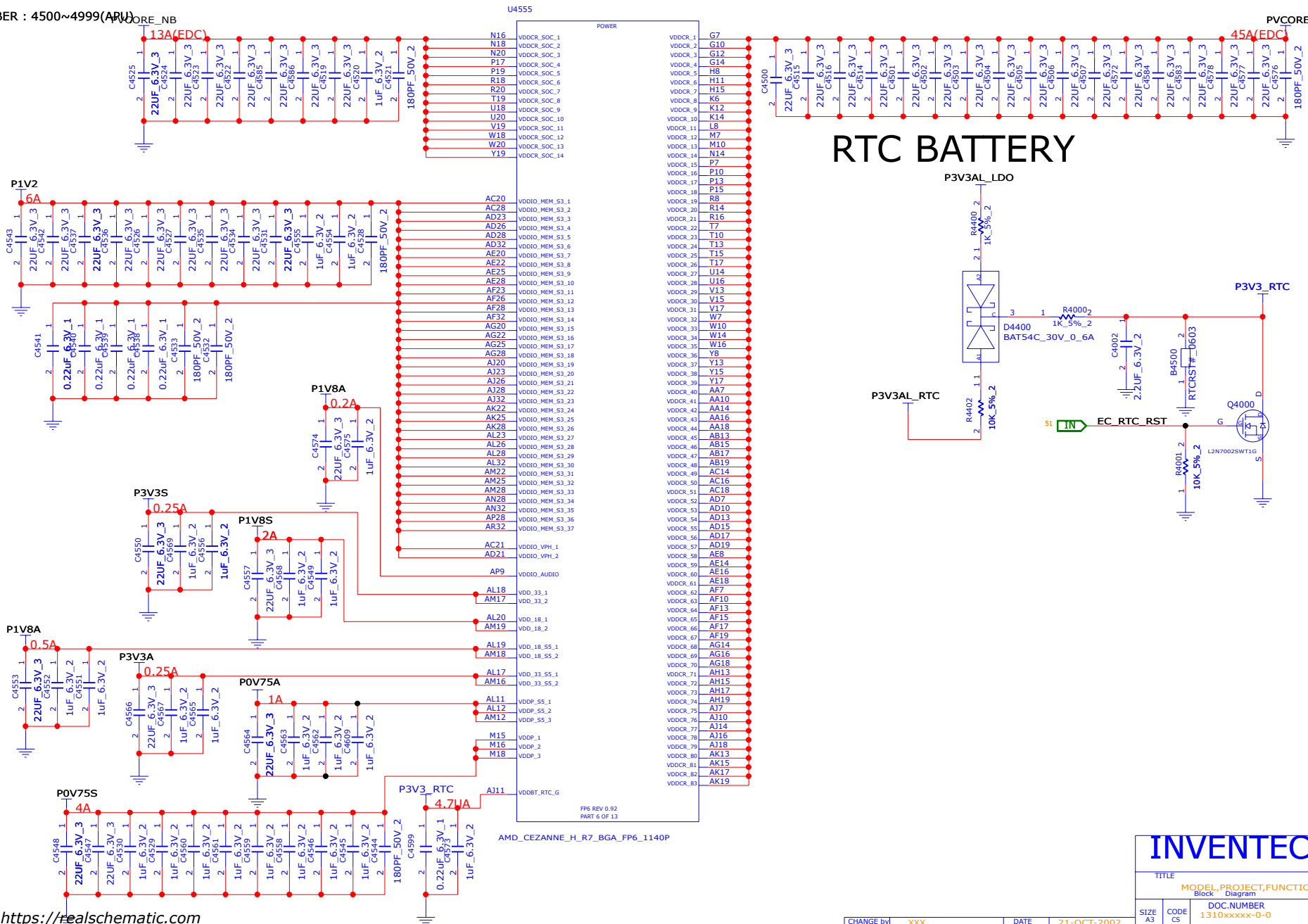
APU_FP6_USB

LOCATION NUMBER : 4500~4999(APU)



APU_FP6_POWER

LOCATION NUMBER : 4500~4999 (APU) CORE_NB



FP6 REV 0.02 PART 6 OF 13

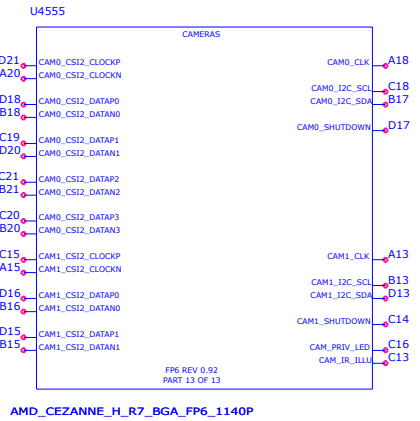
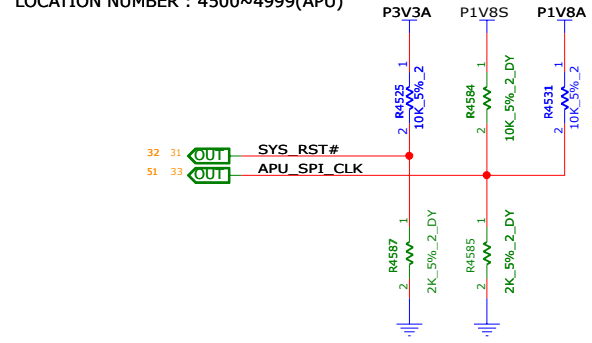
AMD_CEZANNE_H_R7_BGA_FP6_1140P

<https://realschematic.com>

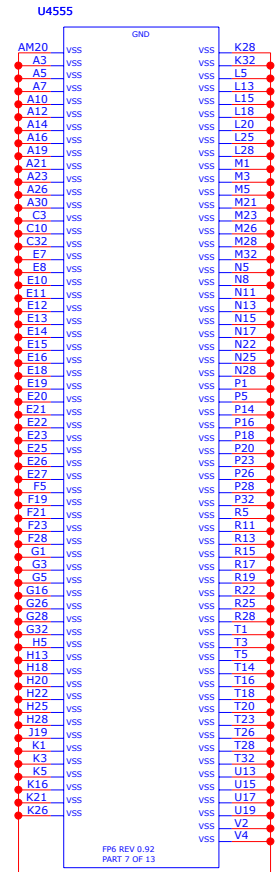
INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 36 of 119	
PCB P/N 60xxxxxxxxxx	PCB VER XXX		

APU_FP6_DGND

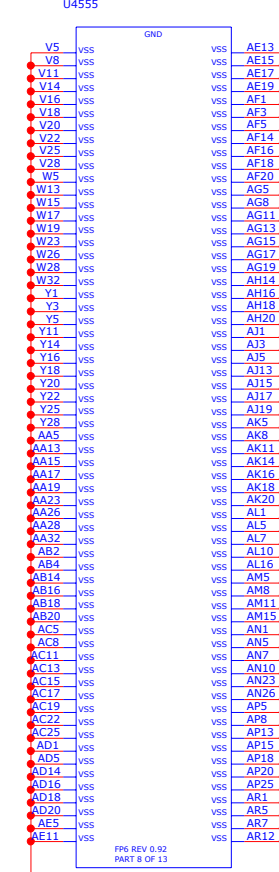
LOCATION NUMBER : 4500~4999(APU)



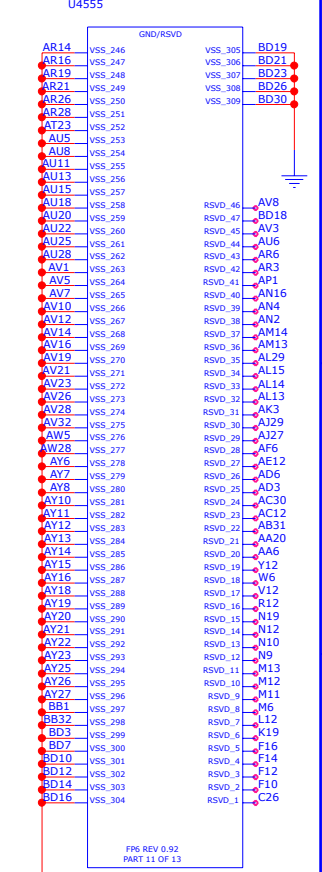
AMD_CEZANNE_H_R7_BGA_FP6_1140P



AMD_CEZANNE_H_R7_BGA_FP6_1140P

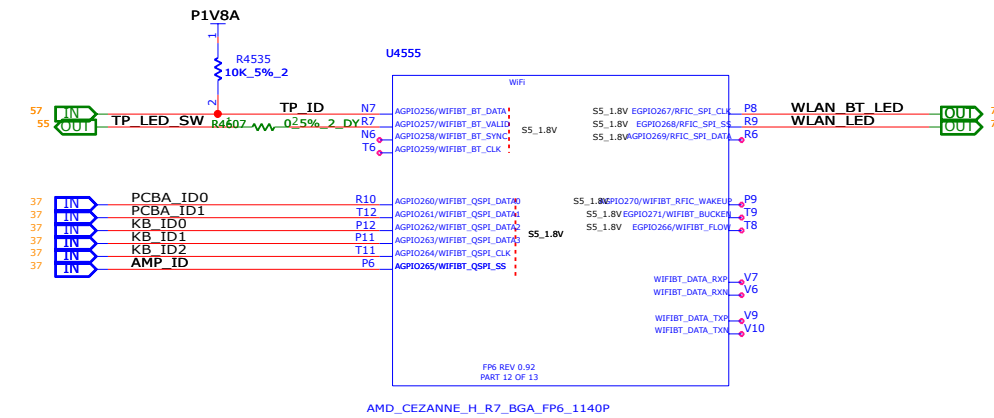


AMD_CEZANNE_H_R7_BGA_FP6_1140P



AMD_CEZANNE_H_R7_BGA_FP6_1140P

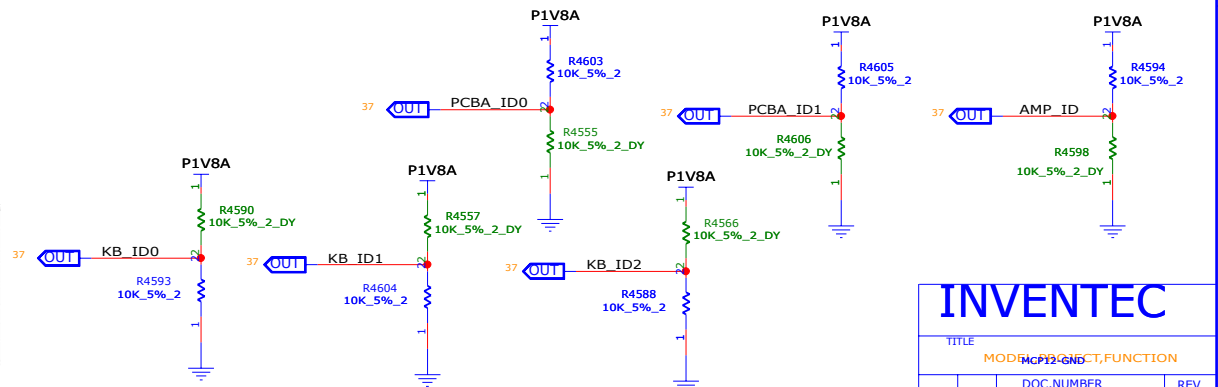
STRAP	DEFINITION
SPI_CLK	1: USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0: USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RST#	1: NORMAL RESET MODE(DEFAULT) 0: SHORT RESET MODE



AMD_CEZANNE_H_R7_BGA_FP6_1140P

AGPIO262/WIFIBT_QSPI_DATA2	AGPIO263/WIFIBT_QSPI_DATA3	AGPIO264/WIFIBT_QSPI_CLK	指配SKU	註解
KB ID0	KB ID1	KB ID2	1,2,3,5	15" 4 Zone
0	0	1	4	15" PerKey
0	1	0	6,7,8,9,10,11,12	15" PerKey RGB
1	0	0	13,14,15,17	17" 4 Zone
1	0	1	16,18,19	17" PerKey
1	1	0	20,21,22,23,24,25,26	17" PerKey RGB

<https://realschematic.com>



INVENTEC

TITLE: **MOD:MCPCB,FUNCTION**

SIZE A3 CODE CS 1310XXXX-0-0 REV X01

CHANGE by PCB #/N DATE PCB VER SHEET 37 of 119

EDP_REDRIIVER

LOCATION NUMBER : 3050~3099

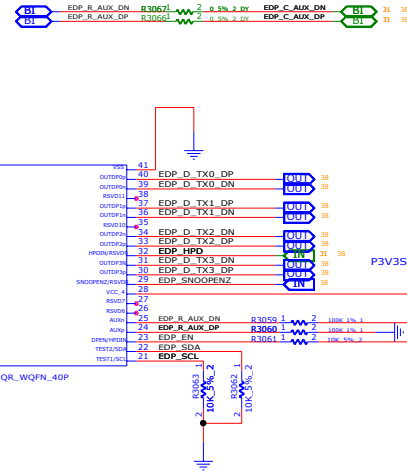
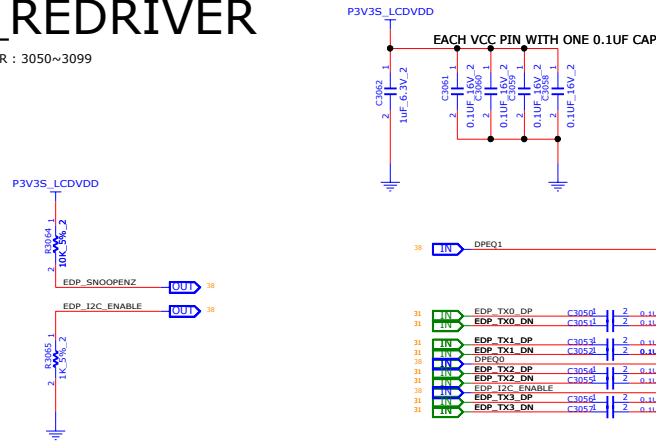


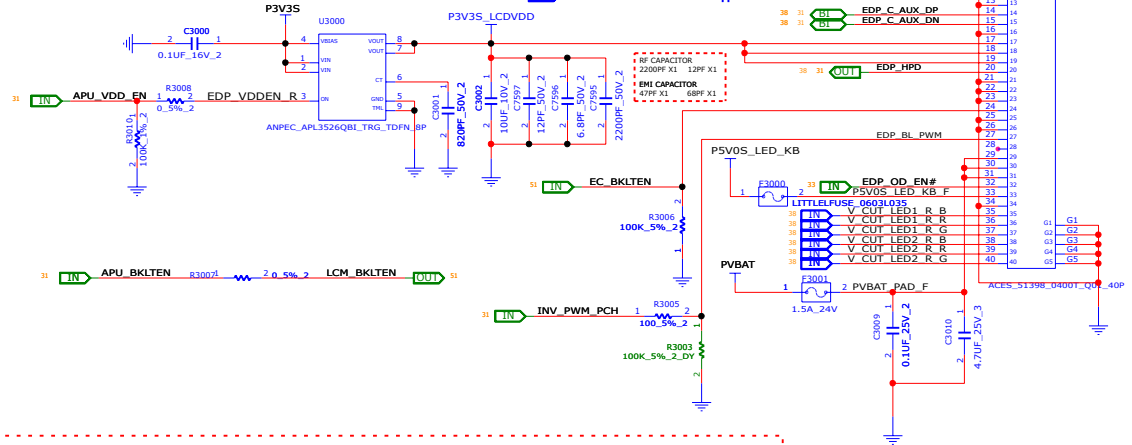
Table 1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Option 1: Tie 1 kΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 kΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 kΩ 5% to V _{CC} . Option 2: Tie directly to V _{CC} .

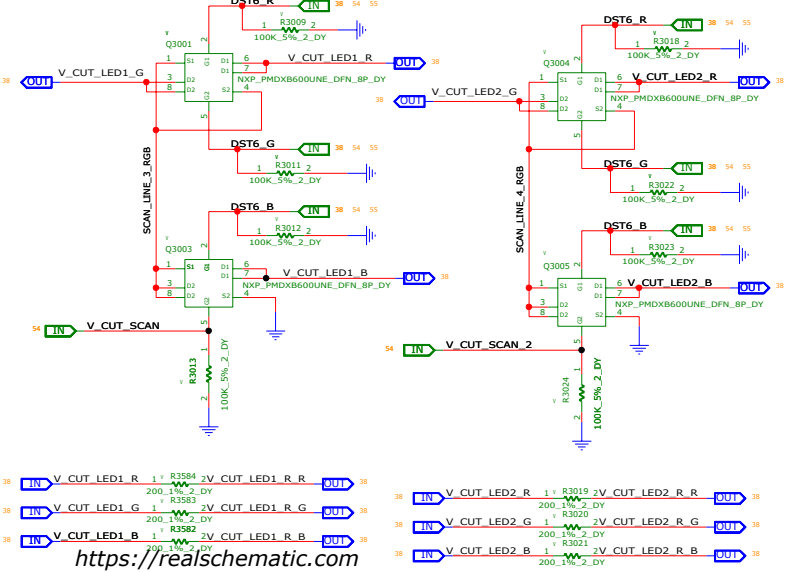
I2C_EN	17	4 Level I	IC Programming Mode or GPIO Programming Select. I2C is only disabled when this pin is '0'. 0 = GPIO mode (IC disabled). R = TI Test Mode (IC enabled at 3.3 V). F = IC enabled at 1.8 V. 1 = IC enabled at 3.3 V.
TESTY/ISCL	21	2 Level I	When I2C_EN=0, pull down with 10k or directly connect to ground. Otherwise this pin is IC clock. When used for IC clock pullup to IC master's VCC IC supply.
TESTZ/SDA	22	2 Level I	When I2C_EN=0, pull down with 10k or directly connect to ground. Otherwise this pin is IC data. When used for IC data pullup to IC master's VCC IC supply.
DPENHPDIN	23	2 Level I (Fail-safe) (PD)	DP Enable Pin. When I2C_EN = '0', this pin will enable or disable DisplayPort functionality. Otherwise, when I2C_EN is not '0', this pin is an input for Hot Plug Detect (HPD) received from DisplayPort sink. When this HPDIN is low for greater than 2 ms, all DisplayPort lanes are disabled. L = DisplayPort Disabled (Pull-down with 10k resistor) H = DisplayPort Enabled (Pull-up with 10k resistor)
AUXp	24	IO, CMOS	This pin along with AUXn is used by the TDP142 for AUX snooping. See the Application and Implementation section for more detail.
AUXn	25	IO, CMOS	This pin along with AUXp is used by the TDP142 for AUX snooping. See the Application and Implementation section for more detail.
SNOOPEZ/RSVD8	29 ⁽²⁾	IO (PD)	When I2C_EN=1, this pin is reserved. When I2C_EN=0, this pin is SNOOPEZ (L=AUX snooper enabled and H=AUX snooper disabled with all lanes active).
HPDIN/RSVD9	32 ⁽²⁾	IO (PD)	When I2C_EN=1, this pin is reserved. When I2C_EN=0, this pin is an input for Hot Plug Detect received from DisplayPort sink. When HPDIN is low for greater than 2ms, all DisplayPort lanes are disabled.

EDP_CNTR

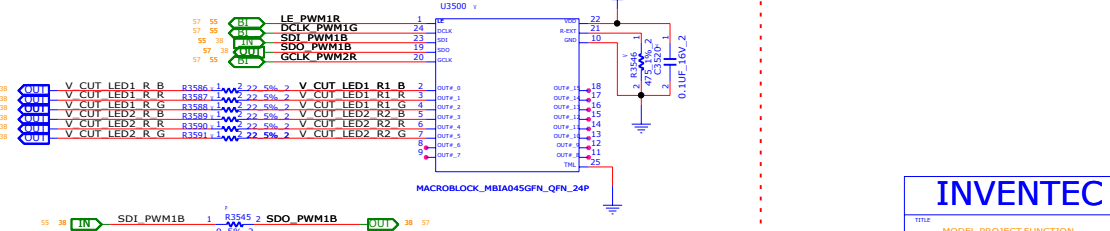
LOCATION NUMBER : 3000~3049



V-CUT LED



V-CUT LED



INVENTEC

TITLE	MODEL_PROJECT/FUNCTION	REV
Block Diagram	13104xxxx-B-B	X01

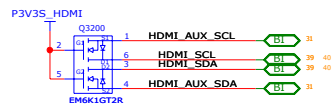
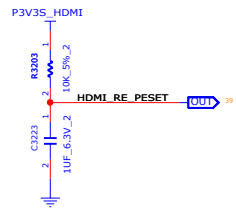
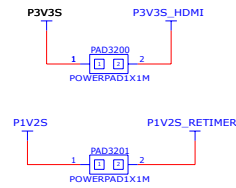
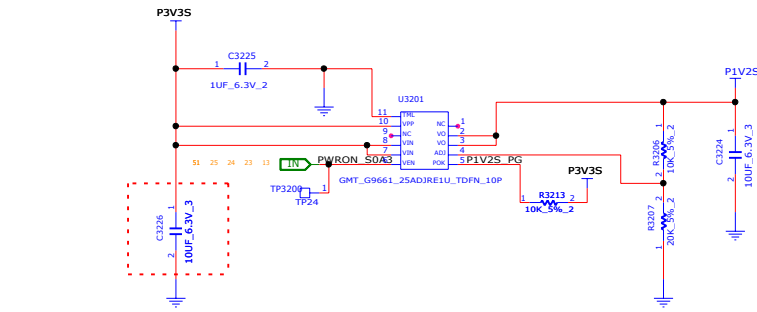
CHANGE BY	DATE	DESCRIPTION
XXX	21-OCT-2002	XXX

SCAR : R3545 DY

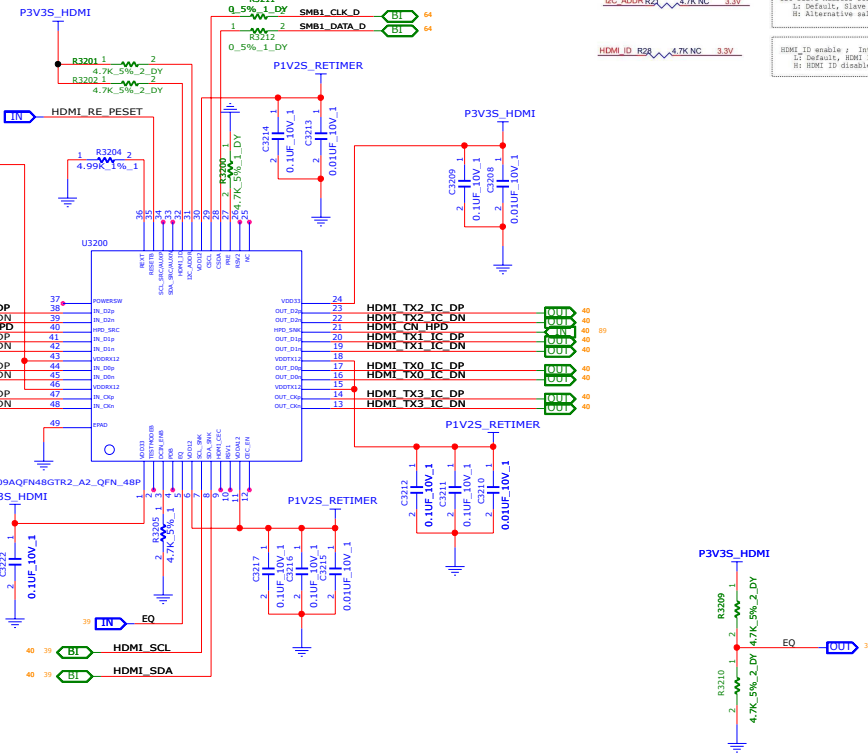
<https://realschematic.com>

HDMI REPEATER PS8409A

LOCATION NUMBER : 3200~3299



I2C ADDR 0X10-0X2F



EQ	R201	4.7K NC	3.3V	Receiver equalization setting: Internal pull up, 3.3V I/O. I: Compensation for channel loss up to 3.18m N: Default, Compensation for channel loss up to 17dB M: Compensation for channel loss up to 11dB
PRE	R1X	4.7K NC	GND	Output pre-emphasis setting: Internal pull up, 3.3V I/O. I: Pre-emphasis 0.25dB N: Default, No Pre-emphasis
I2C_ADDR	R21	4.7K NC	3.3V	I2C Slave Address selection: Internal pull down, 3.3V I/O. I: Default, Slave address 0x10-0x2F N: Alternative slave address 0x90-0x9F, 0x20-0x2F.
HDMI_ID	R28	4.7K NC	3.3V	HDMI_ID enable : Internal pull down, 3.3V I/O. I: Default, HDMI_ID enable N: HDMI_ID disable

<https://realschematic.com>

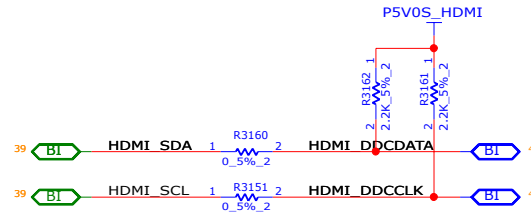
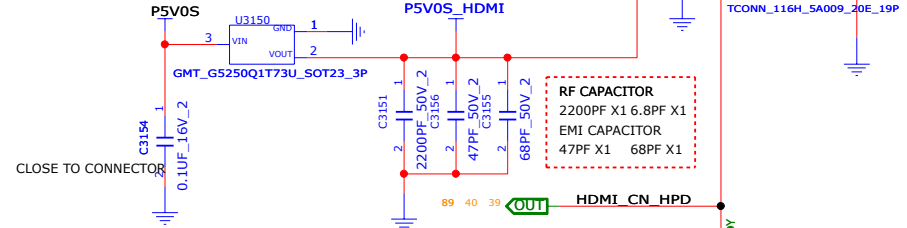
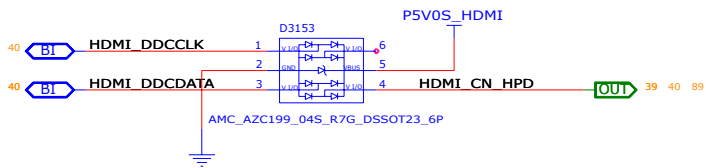
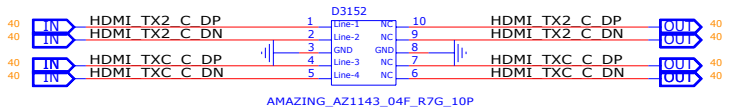
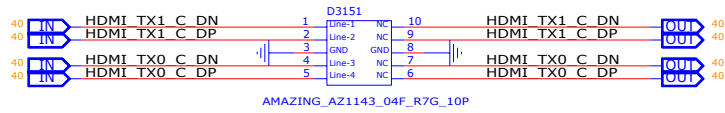
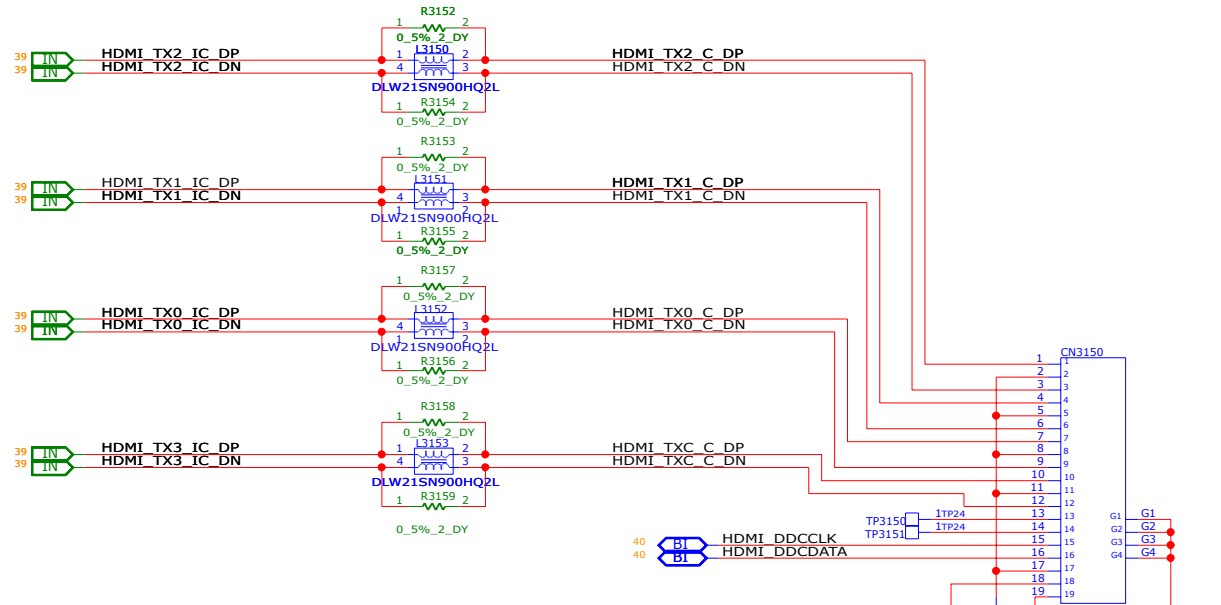
INVENTEC

TITLE	MODEL_PROJECT/FUNCTION
Block	Diagram
SIZE	CODE
A2	CS
SHEET	33 of 116
DATE	21-OCT-2002
DATE	21-OCT-2002
REV	1.0
REV	1.0

CHANGE BY	XXX	DATE	21-OCT-2002
PCB P/N	6PXXXXXXXXXXXX	PCB VER	XXX

HDMI CONN

LOCATION NUMBER : 3150~3199



<https://realschematic.com>

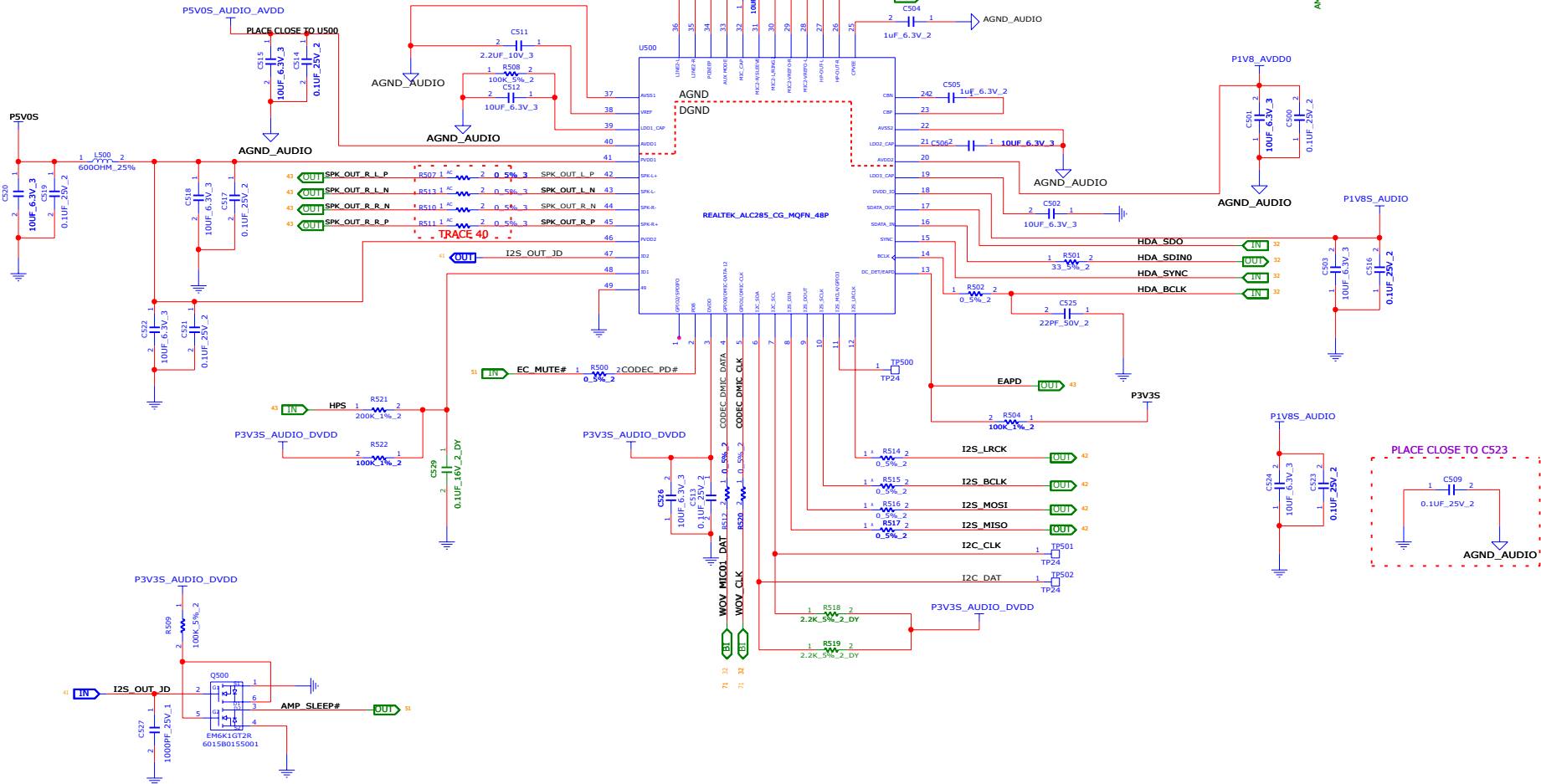
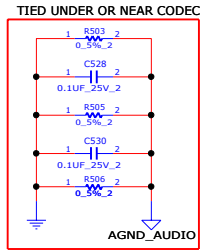
INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET		40 of 119	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

AUDIO CODEC ALC295

LOCATION NUMBER : 500~549



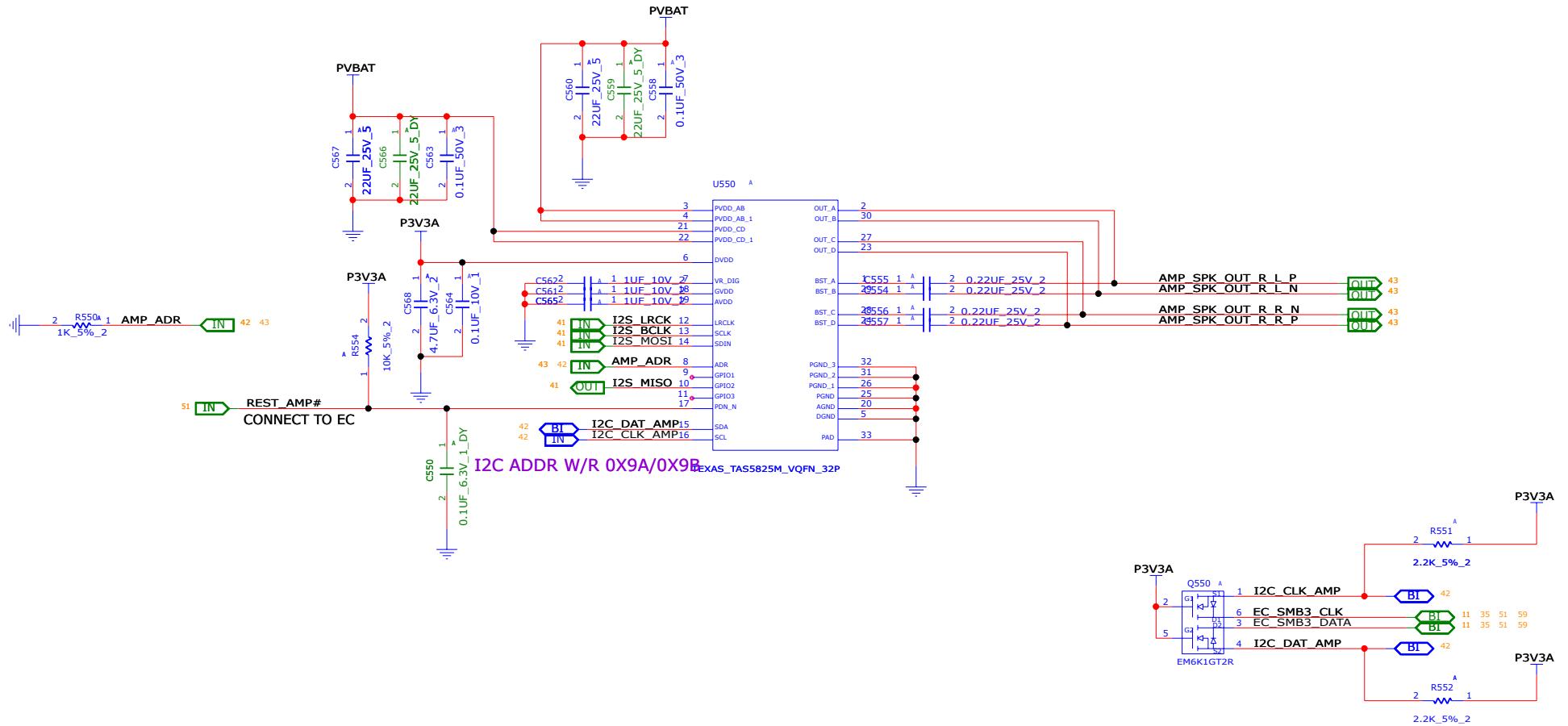
LOCATION NUMBER:500~699

<https://realschematic.com>

INVENTEC			
MODEL_PROJECT_FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A1	CS	133100000000-0	1.0
CHANGE IN		DATE	21-OCT-2002
PCB P/N		PBR VER	XXX
SHEET		11	116

AUDIO AMP TI TAS5825M FOR X60/SCAR

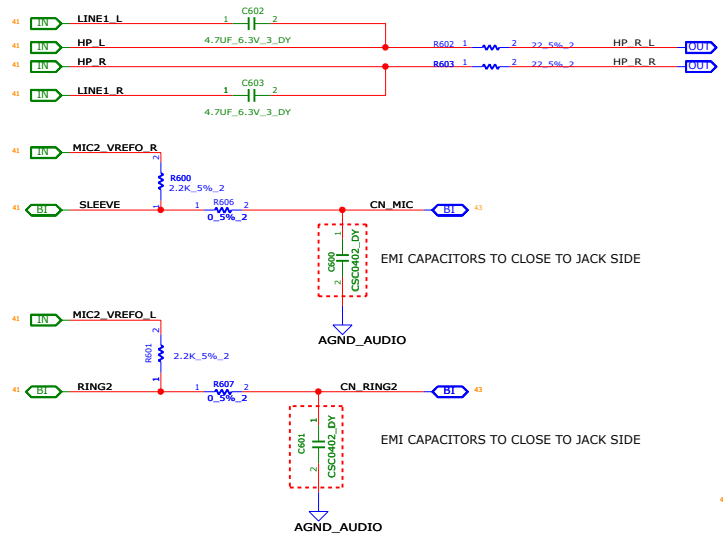
LOCATION NUMBER : 550~599



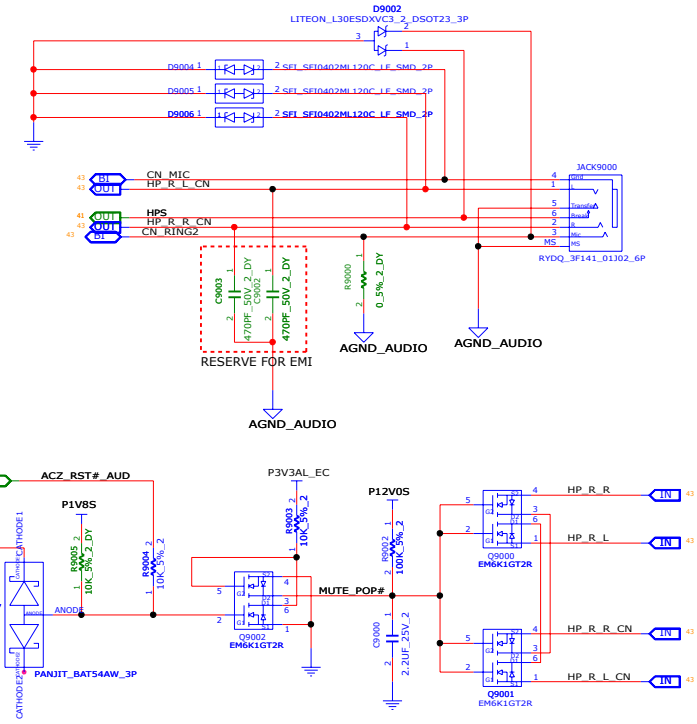
AUDIO SPK/JACK

LOCATION NUMBER : 600~699(SPK)
LOCATION NUMBER : 9000~9099(JACK)

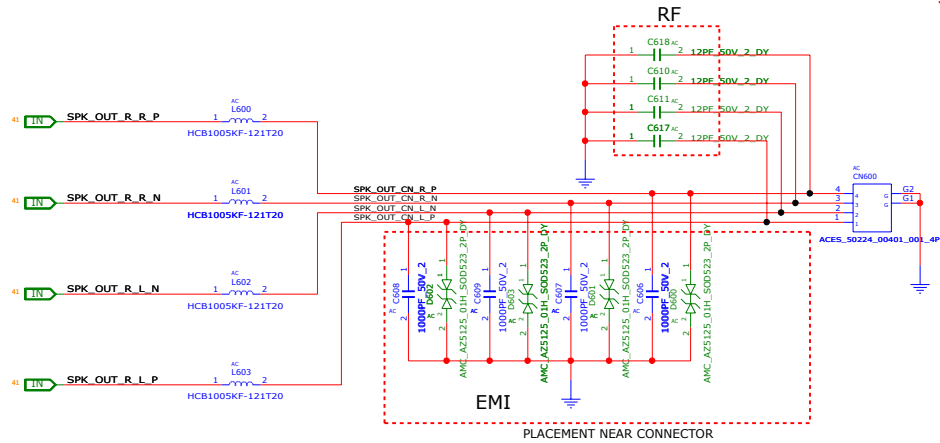
CODEC SIDE



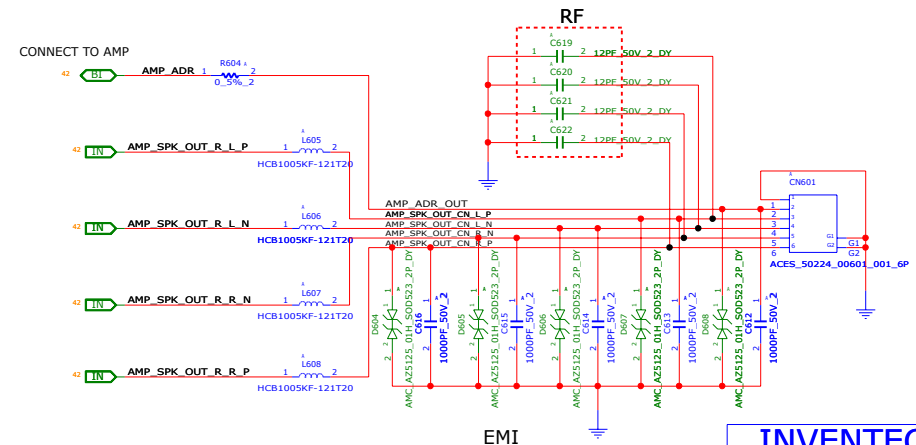
AUDIO JACK



AUDIO CODEC SPEAKER



AUDIO SMART AMP SPEAKER



<https://realschematic.com>

INVENTEC

TITLE		MODEL/PROJECT/FUNCTION		REV	
Block Diagram				131000xxxx-0-0	
CHANGE IN	XXX	DATE	21-OCT-2002	SIZE	A1
Pcb Pin	6Pxxxxxx	Pcb Ver	xxx	SHEET	41 of 110

RESERVE

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

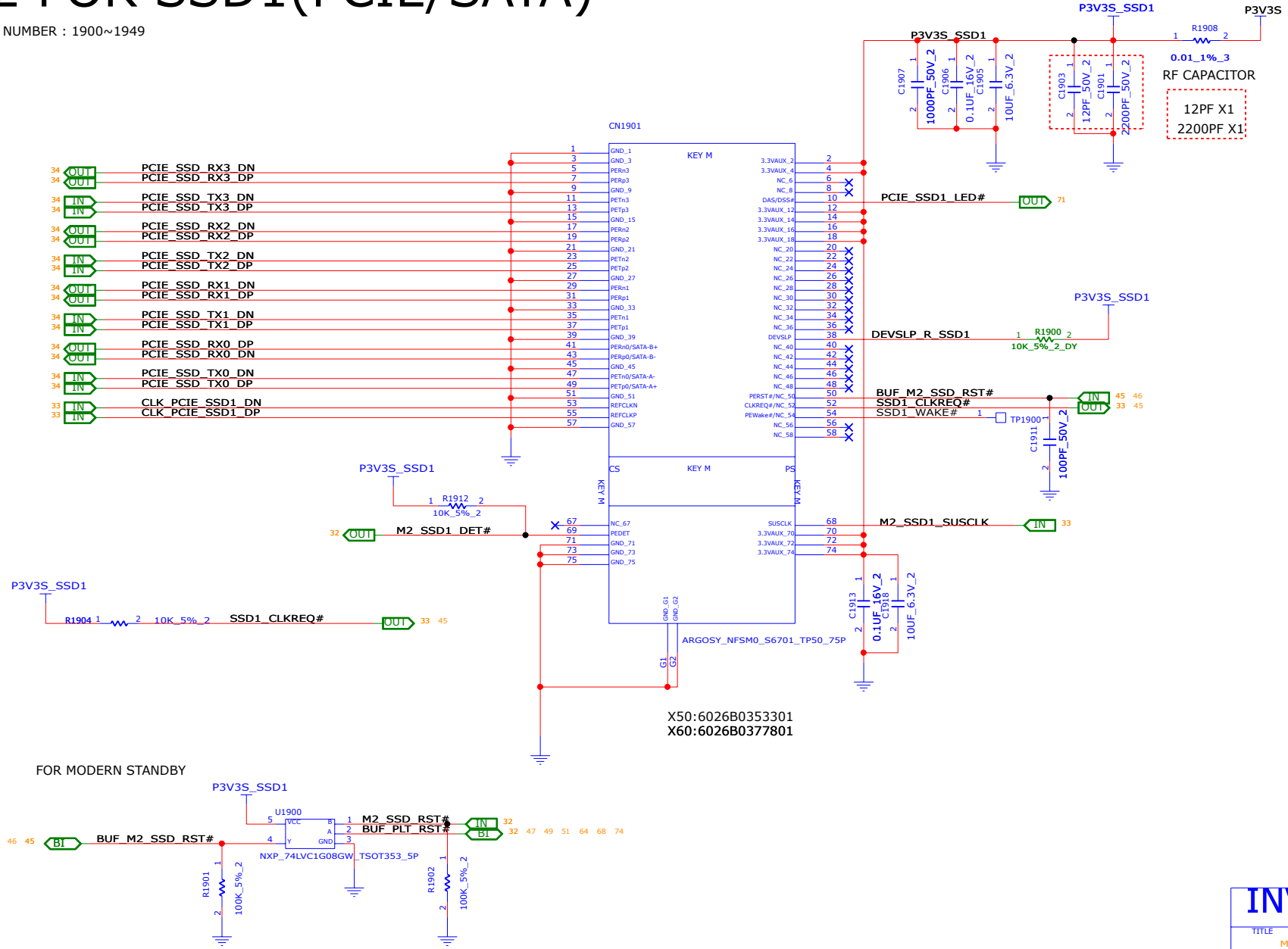
SIZE CODE DOC.NUMBER REV
A3 CS 1310xxxxx-0-0 X01

SHEET 44 of 119

CHANGE by: XXX DATE: 21-OCT-2002
PCB P/N: 60xxxxxxxxxxx PCB VER: XXX

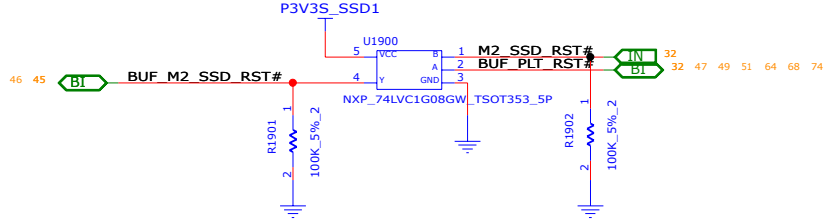
M.2 FOR SSD1(PCIE/SATA)

LOCATION NUMBER : 1900~1949



X50:6026B0353301
X60:6026B0377801

FOR MODERN STANDBY

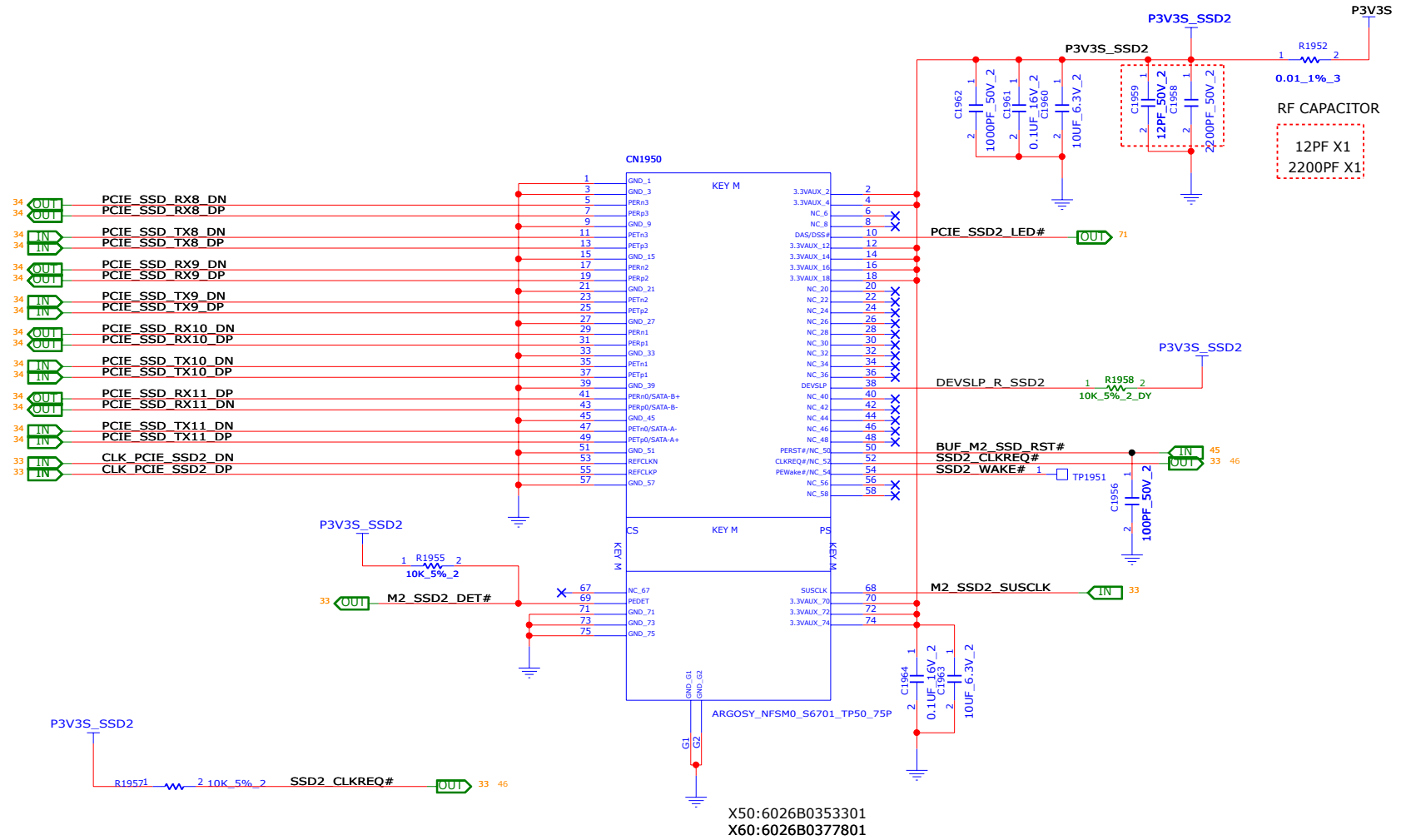


<https://realschematic.com>

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	PCB VER XXX	SHEET 45 of 119
PCB P/N			

M.2 FOR SSD2(PCIE/SATA)

LOCATION NUMBER : 1950~1999



X50:6026B0353301
X60:6026B0377801

INVENTEC

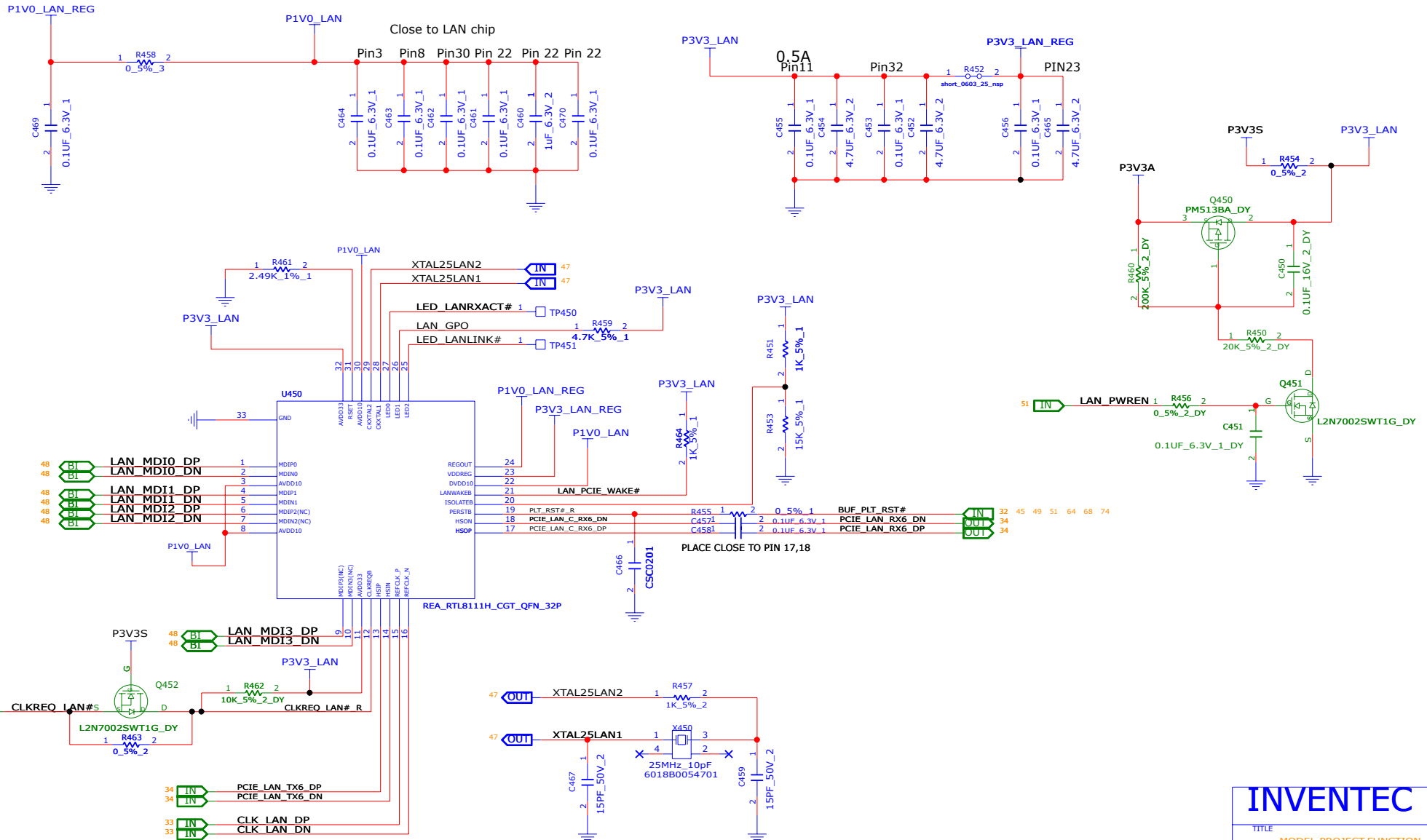
TITLE			
MODEL_PROJECT.FUNCTION			
SATA_HDDCONN.			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET		46 of 119	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

LAN (RTL8111H)

LOCATION NUMBER : 450 ~ 479

P3V3_LAN RISING TIME (10%~90%)要>0.5MS AND <100MS
 LAN POWER NOISE P3V3_LAN < 200MV VPEAK TO VPEAK.
 LAN POWER NOISE P1V0_LAN < 100MV VPEAK TO VPEAK.



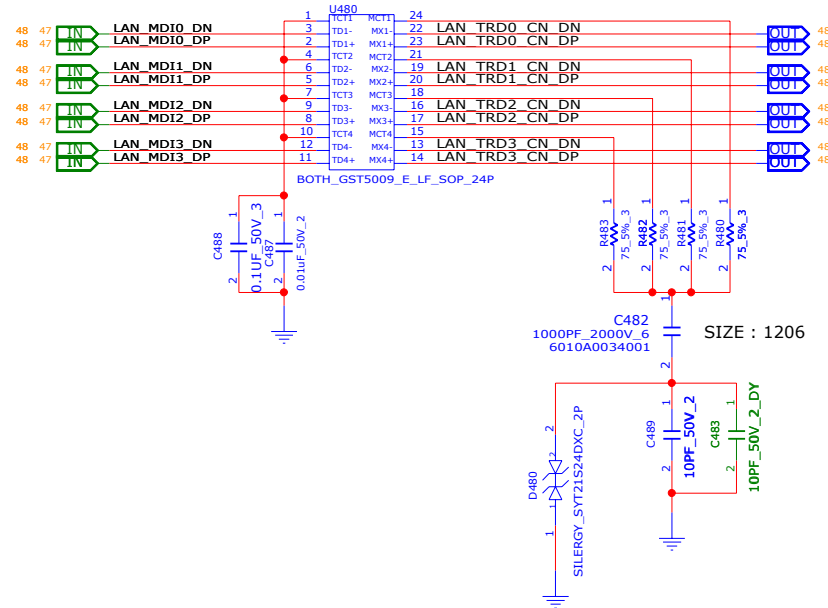
<https://realschematic.com>

INVENTEC			
TITLE			
MODEL_PROJECT_FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
SHEET 47 of 119			

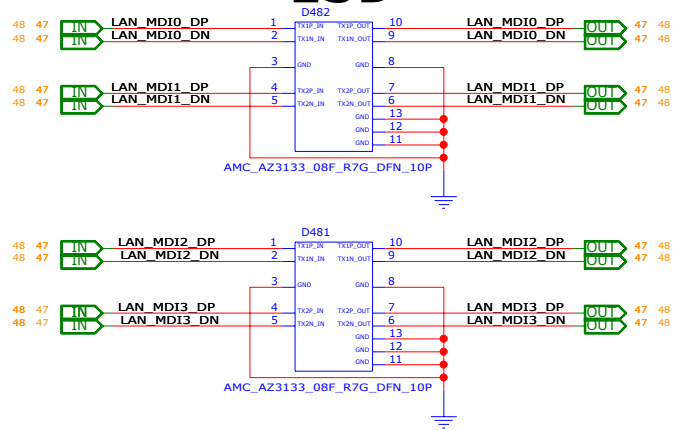
LAN (RTL8111H)

LOCATION NUMBER : 480 ~ 499

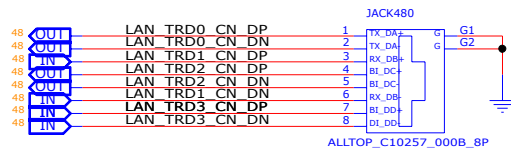
TRANSFORMER



ESD



RJ-45



INVENTEC

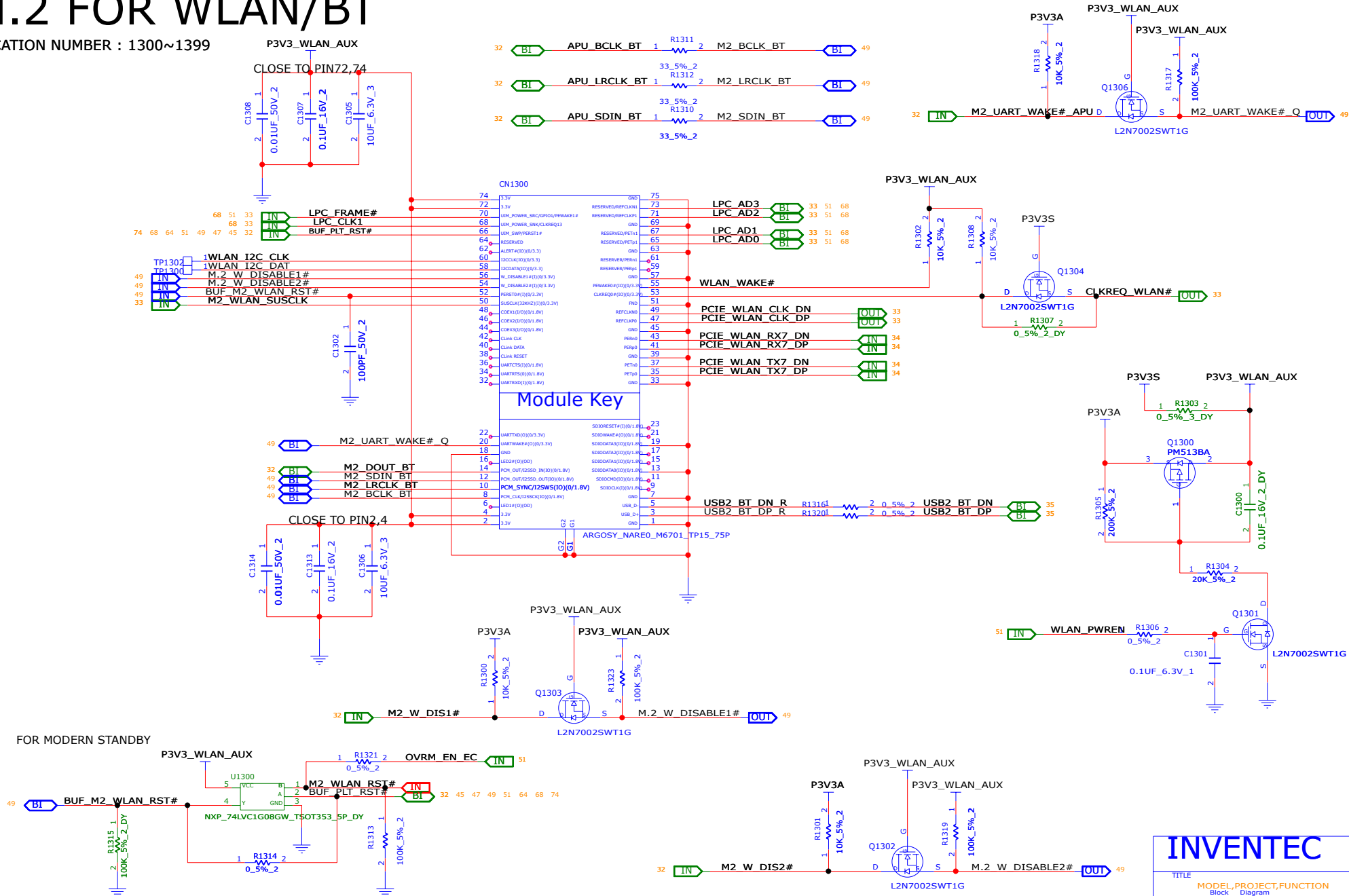
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET		48 of 119	

<https://realschematic.com>

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

M.2 FOR WLAN/BT

LOCATION NUMBER : 1300~1399



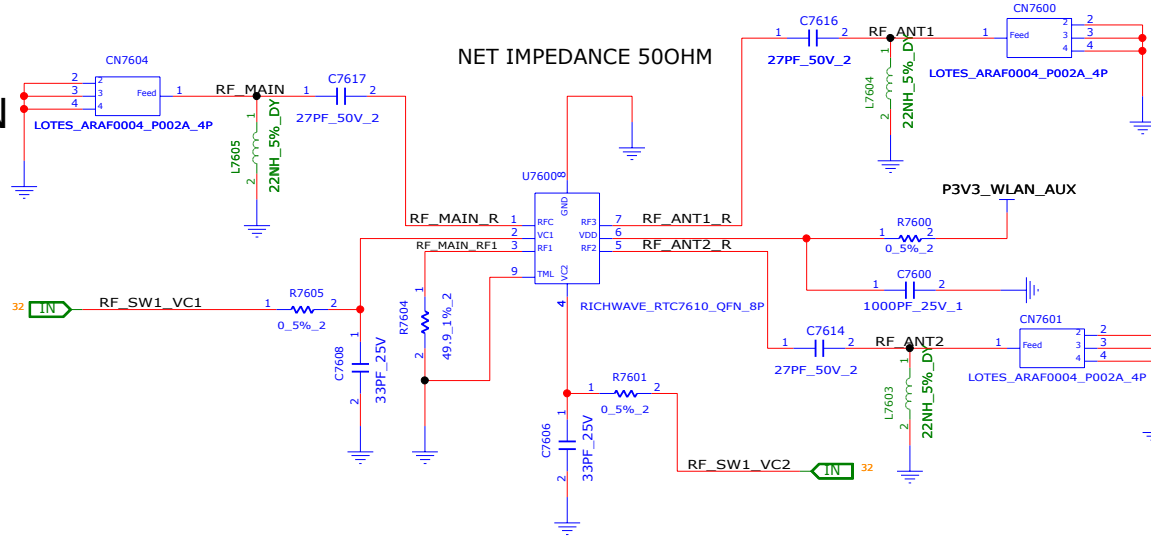
INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER	REV
		1310xxxxx-0-0	X01
CHANGE by		DATE	
PCB P/N		PCB VER	
XXX		21-OCT-2002	
60xxxxxxxxxx		XXX	
SHEET			49 of 119

RF CONN

LOCATION NUMBER : 7600~7699

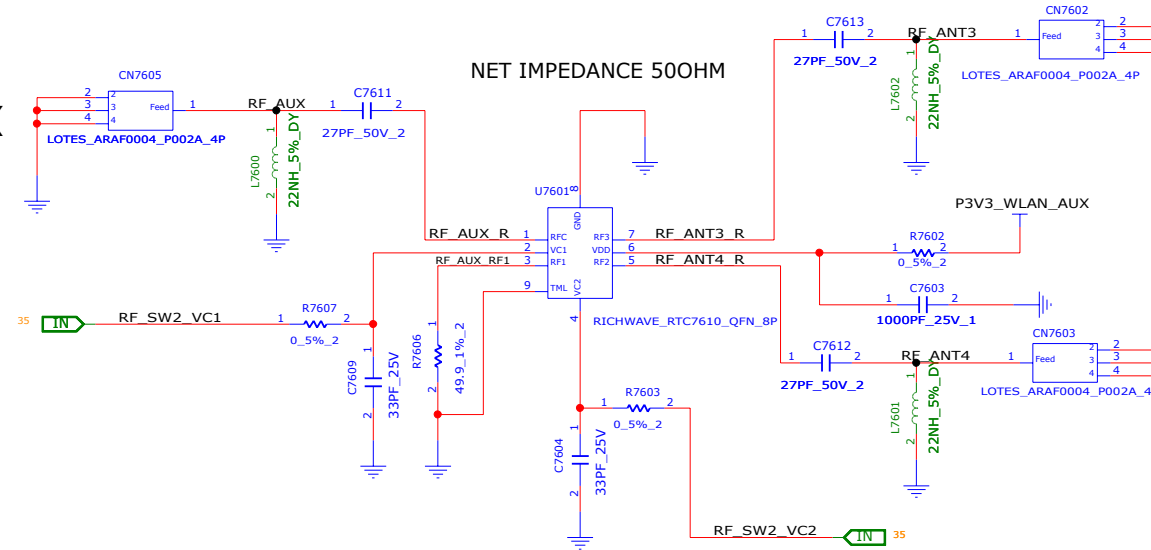
MODULE MAIN



ANT1

ANT2

MODULE AUX



ANT3

ANT4

<https://realschematic.com>

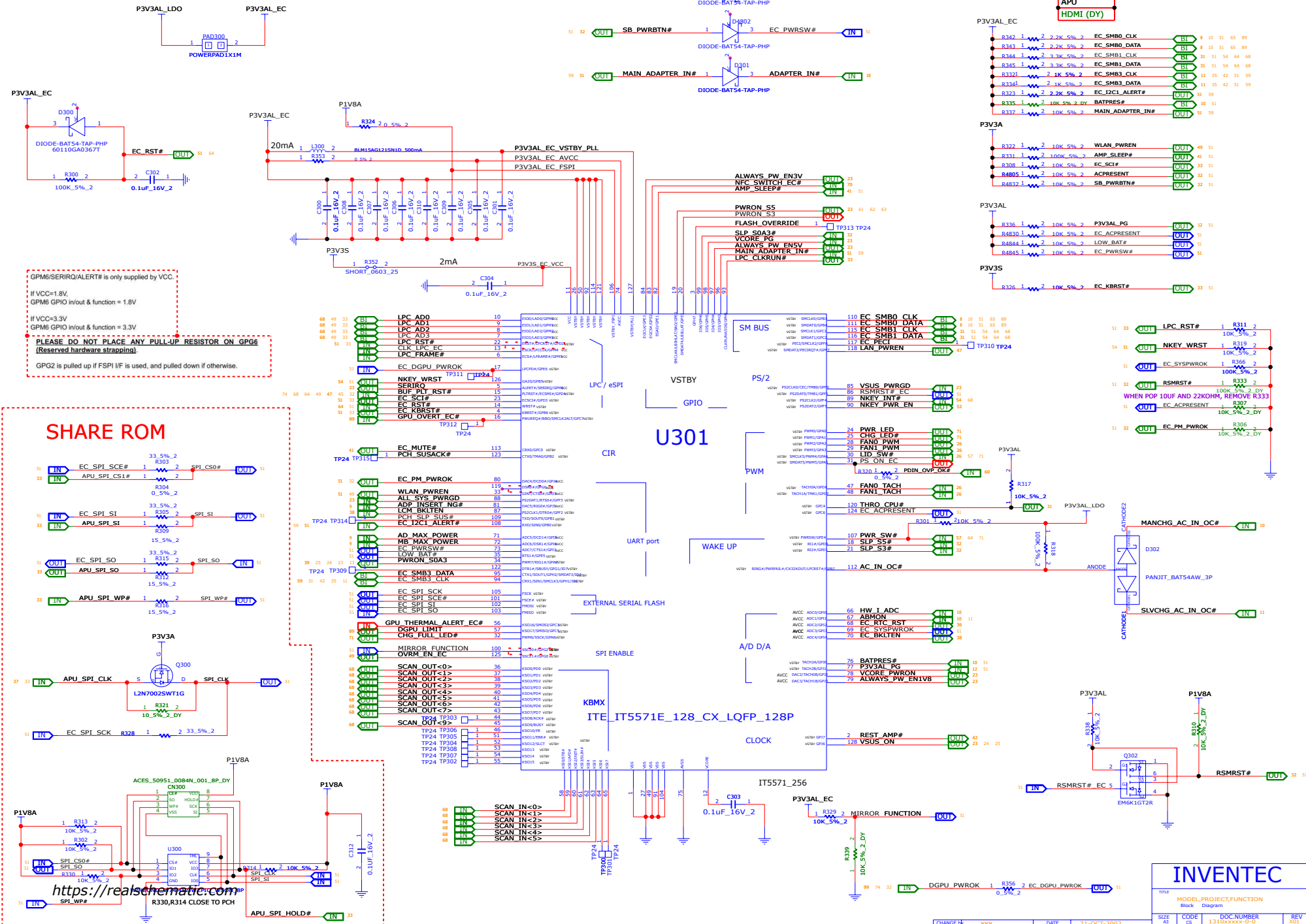
INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET		50 of 119	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

EMBEDDED CONTROLLER IT5571E-C

LOCATION NUMBER : 300~399



GPMS/SERIRQ/ALERT# is only supplied by VCC.
 If VCC=1.8V
 GPMS GPIO in/out & function = 1.8V
 If VCC=3.3V
 GPMS GPIO in/out & function = 3.3V
PLEASE DO NOT PLACE ANY PULL-UP RESISTOR ON GPMS
 (Reserved hardware strapping)
 GP2Z is pulled up if FSPI I/F is used, and pulled down if otherwise.

SHARE ROM

EC_SPI_SCE# 1 R303
 APU_SPI_CS1# 1 R304
 EC_SPI_SI 1 R305
 APU_SPI_SI 1 R306
 EC_SPI_SO 1 R307
 APU_SPI_SO 1 R308
 APU_SPI_WP# 1 R309

P3V3A
 L2N7002SWT1G
 R321 1 10.5%_2_DY
 EC_SPI_SCK R328 1 33.5%_2

P1V8A
 ACES_50951_0884N_001_BP_DY
 C300
 R313 1 10K_5%_2
 R302 1 10K_5%_2
 R310 1 10K_5%_2
 R311 1 10K_5%_2
 R312 1 10K_5%_2
 R314 1 10K_5%_2

APU_SPI_HOLD#

INVENTEC

MODEL PROJECT FUNCTION
 Block Diagram

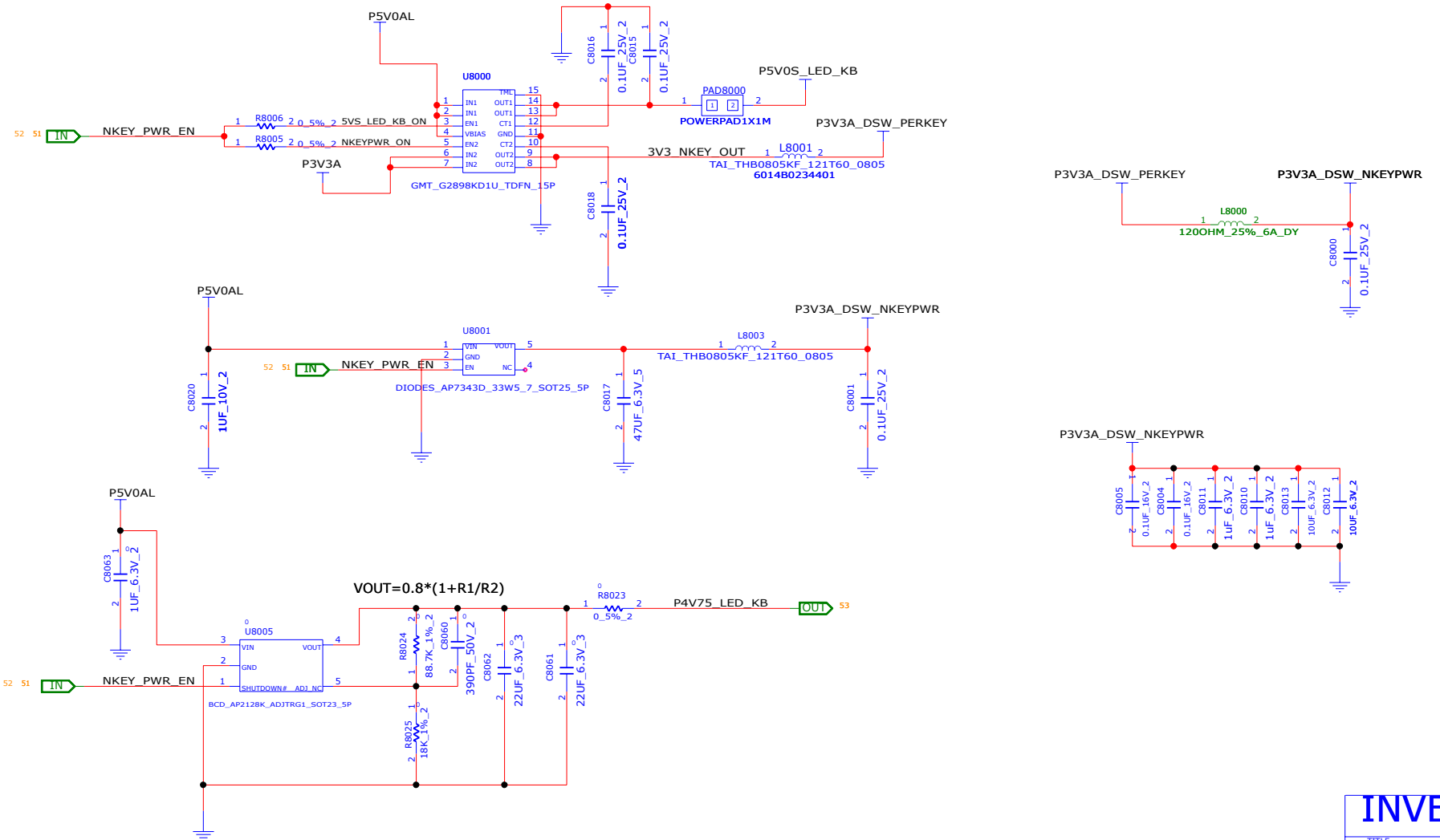
SIZE A1 CODE 1.33.00000000-0
 DOC NUMBER 111
 REV 001

CHANGE I/ PCB P/N XXX
 DATE 21-OCT-2002
 PCB VER XXX

<https://realschematic.com>

NKEY_POWER

LOCATION NUMBER : 8000~8199



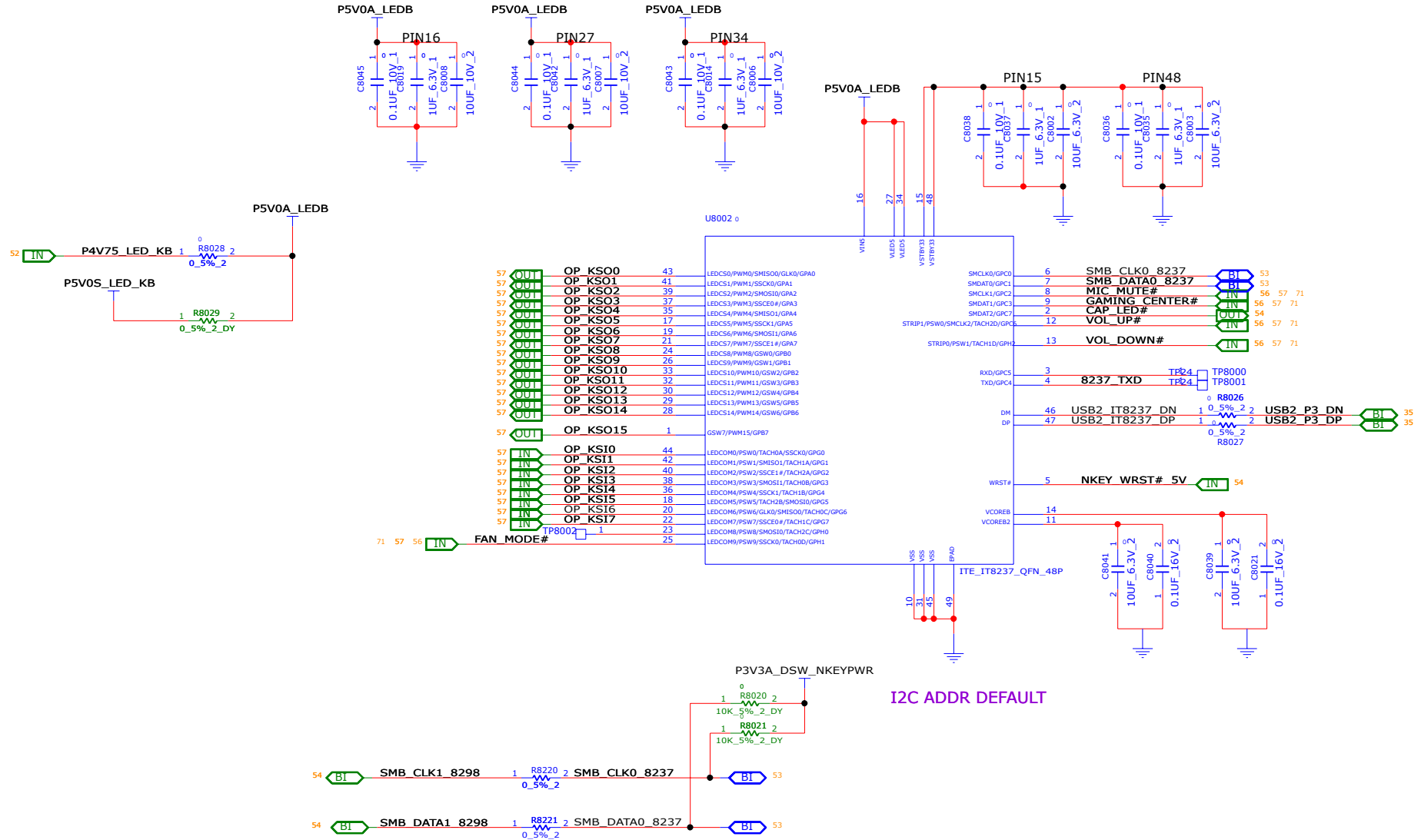
<https://realschematic.com>

INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
SHEET 52 of 119			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX
SIZE A3	CODE CS	DOC. NUMBER	1310xxxxx-0-0
SHEET	52 of 119	REV	X01

IT8237

LOCATION NUMBER : 8000~8199



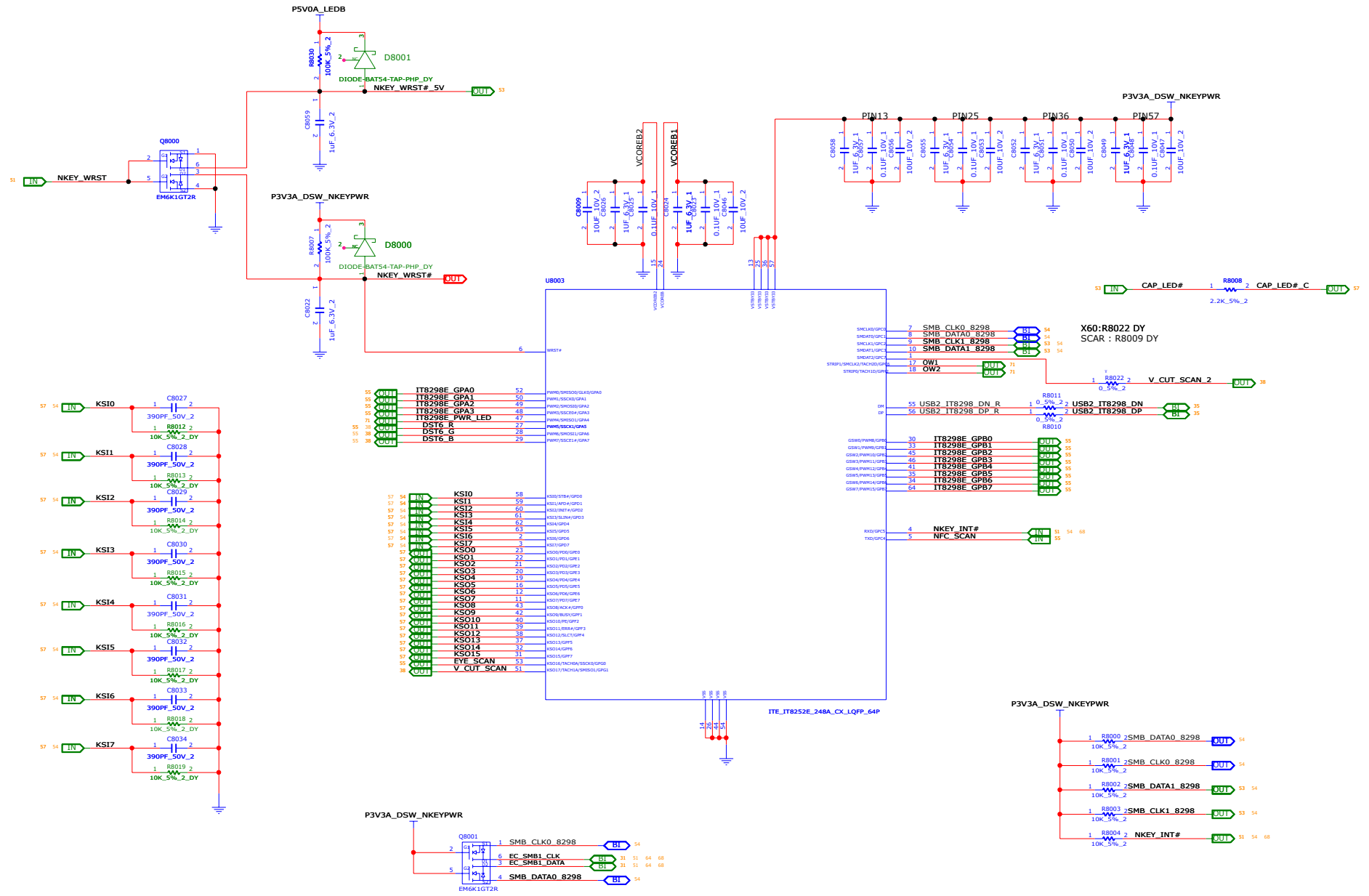
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	
PCB P/N 60xxxxxxxxxx		PCB VER XXX	
SHEET 53 of 119			

IT8252E

LOCATION NUMBER : 8000~8199



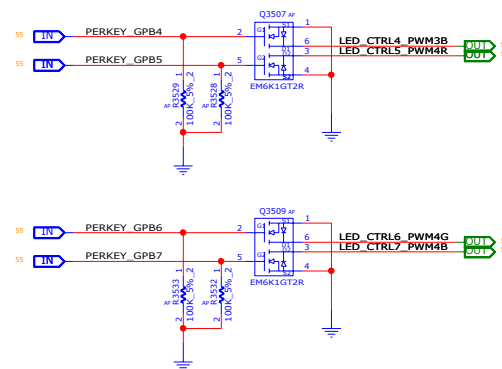
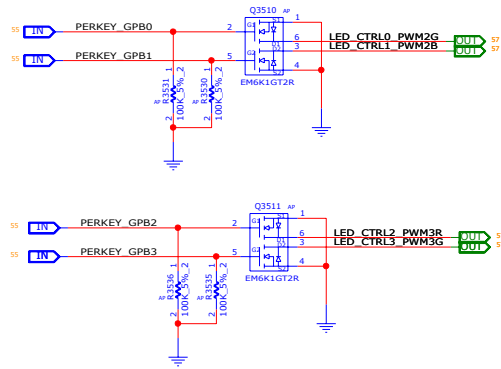
INVENTEC

TITLE	Block	MODEL_PROJECT/FUNCTION	DOC NUMBER	REV
	Diagram		1310xxxxx-B-B	X01
CHANGE BY	XXX	DATE	21-OCT-2002	
PCB P/N	6Pxxxxxxx	PCB VER	XXX	
SIZE A1	CS	SHEET	54 of 110	

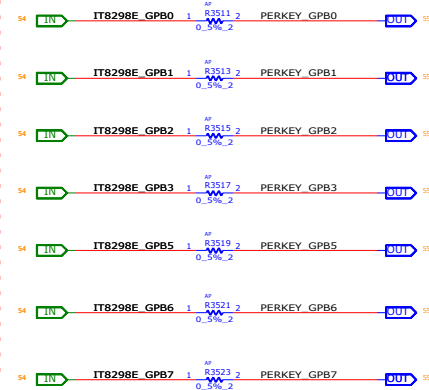
KB/EAGLE EYE RGB LED

LOCATION NUMBER : 3500~3599

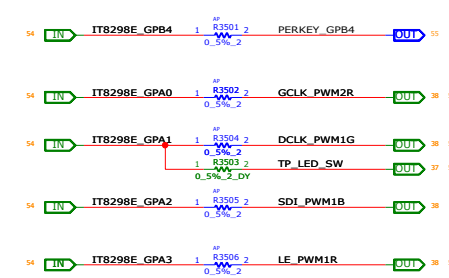
KB RGB PER KEY LED MAX:960MA



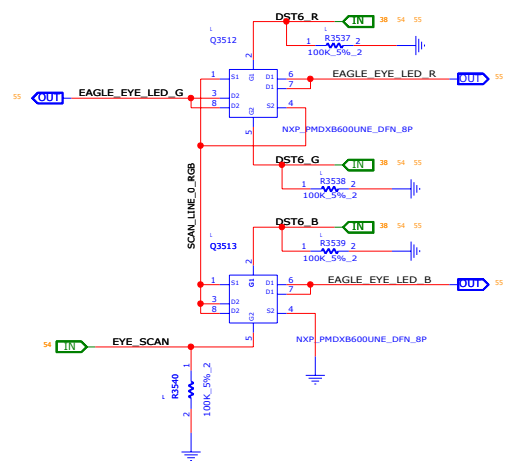
SCAN LINE



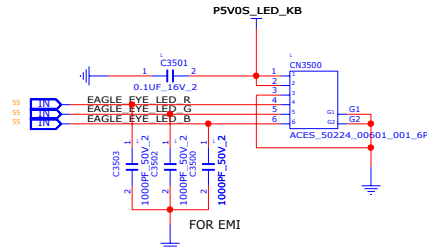
LAUNCH KEY



EAGLE EYE LED MAX:525MA



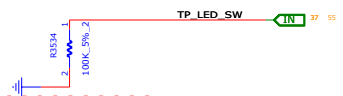
EAGLE EYE LED CONN



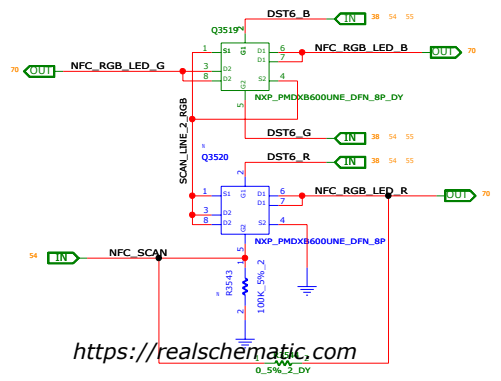
KB RGB 4ZONE LED

MAX:494.5MA

TP LED



NFC RGB LED



<https://realschematic.com>

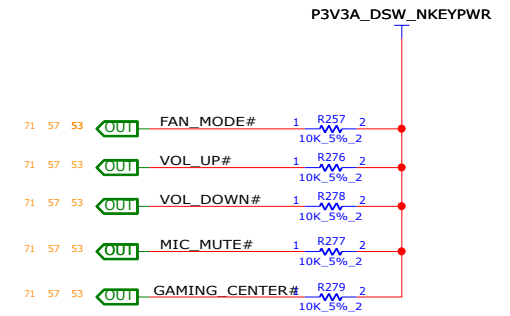
INVENTEC

CHANGE IN		DATE	DOC NUMBER		REV
PCB P/N		PBR VER	1310xxxxx-B-B		X01
SHEET		55 of 110			

IT8013

LOCATION NUMBER : 250~279

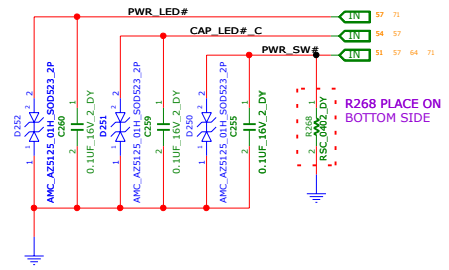
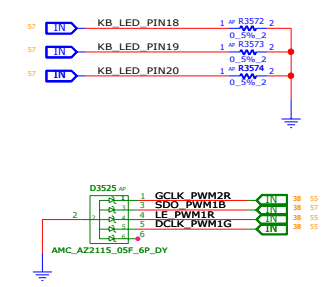
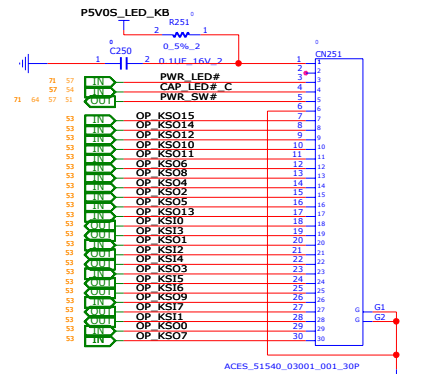
IT8013	LED TYPE SELECT 3V3	KB Type
GP5	H	PerKey
GP5	L	4 Zone/1 Zone RGB



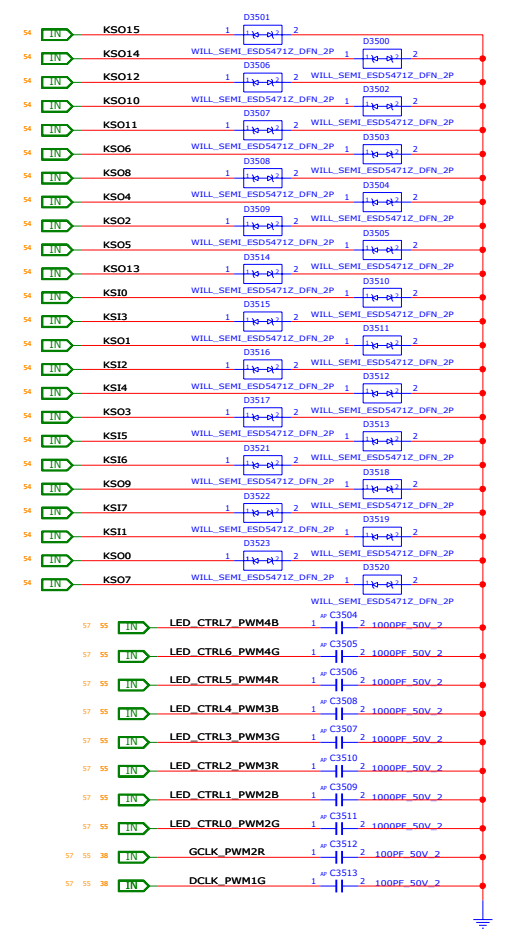
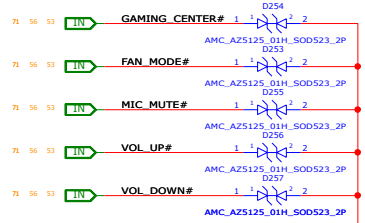
KB CNTR/TOUCH PAD

LOCATION NUMBER : 250~279(KEYBOARD)
 LOCATION NUMBER : 280~299(TP CNTR)

KEYBOARD CONN

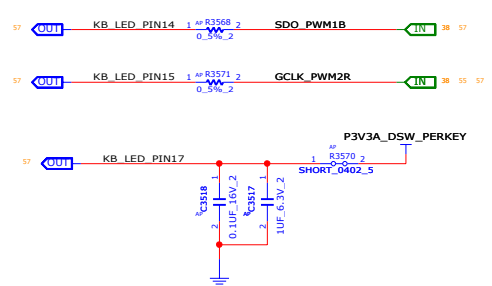
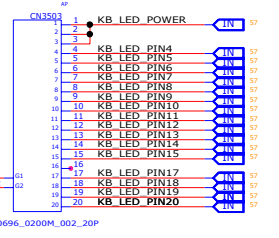


R268 PLACE ON BOTTOM SIDE

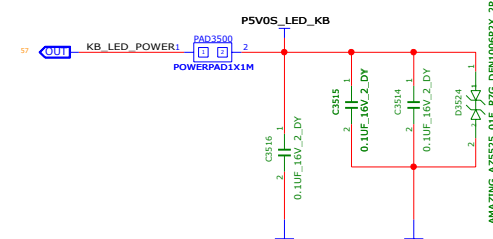


KEYBOARD BACKLIGHT

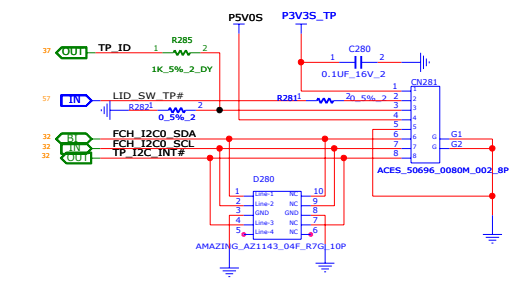
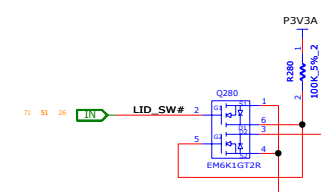
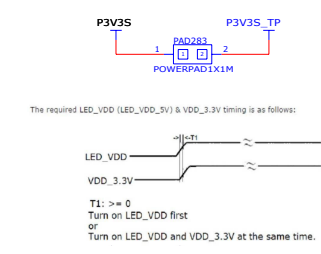
PERKEY



4ZONE



TOUCHPAD



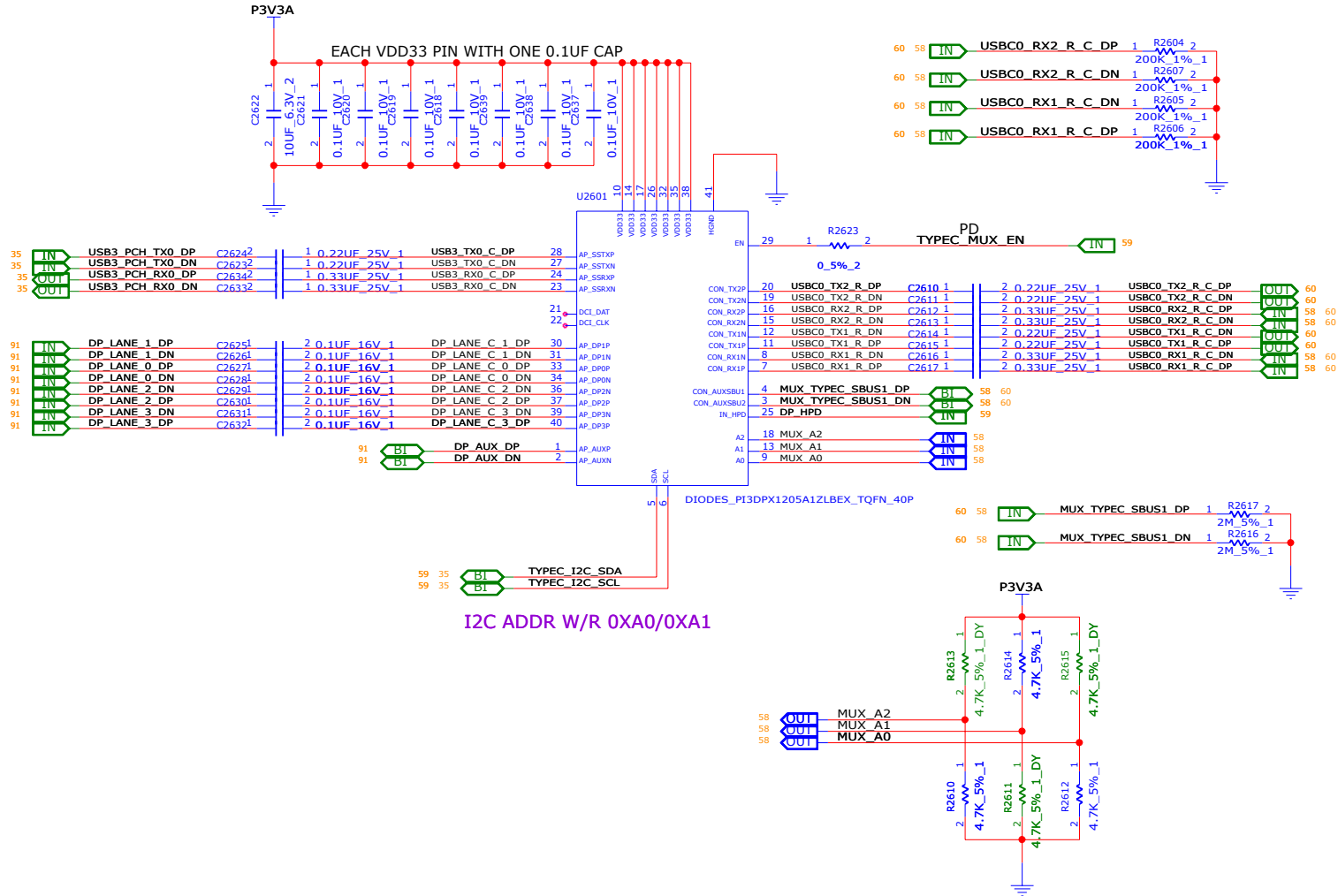
<https://realschematic.com>

INVENTEC

CHANGE ID	XXX	DATE	21-OCT-2002	SIZE	CODE	DOC NUMBER	REV
P/CB P/N	6PXXXXXXXXXX	P/CB VER	XXX	SHEET	57	116	

TYPEC REDRIVER

LOCATION NUMBER : 2600~2699



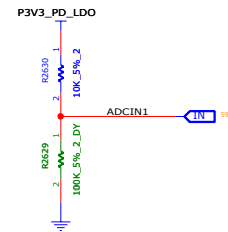
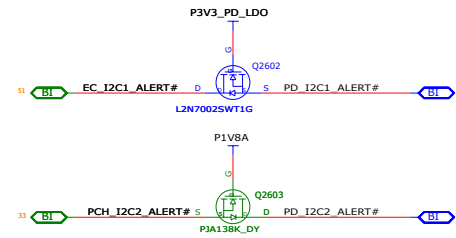
USB TYPE-C PD TPS65993

LOCATION NUMBER : 2600~2699

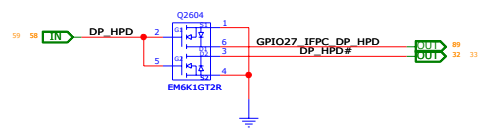
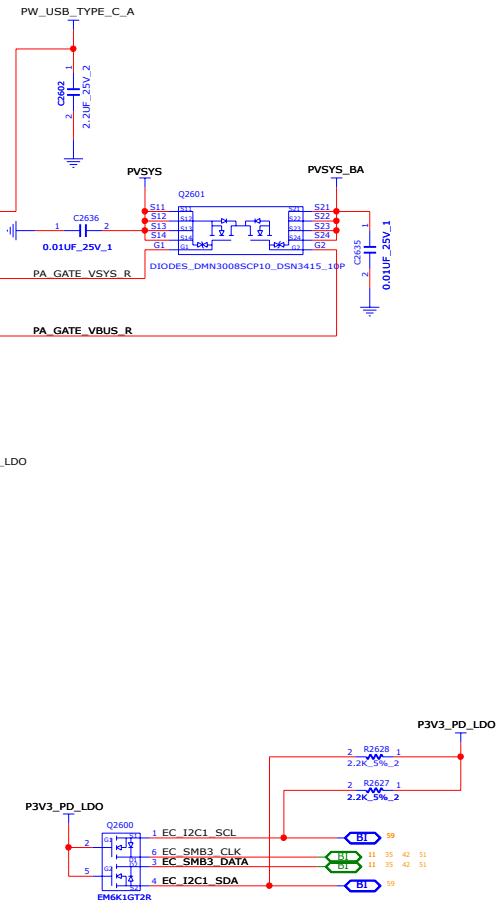
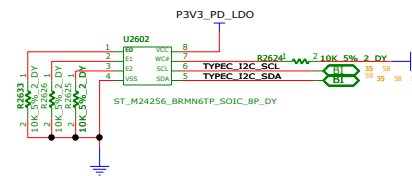
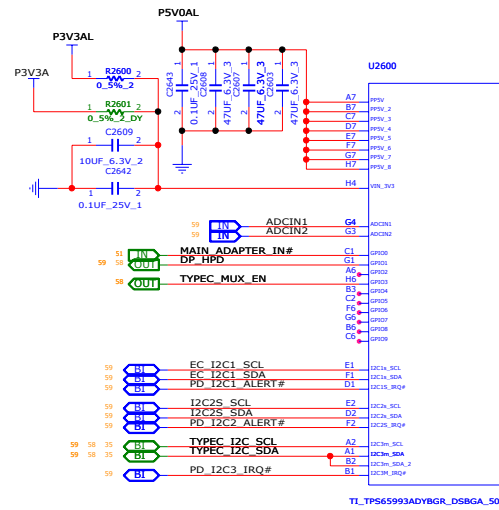
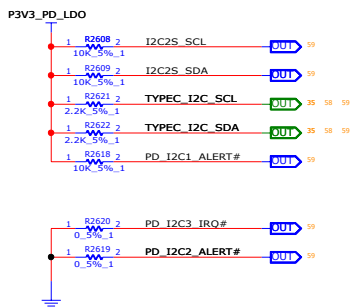
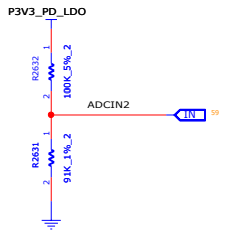
Table 2. Decoding of ADCIN1 and ADCIN2 Pins

DIV = R _{DOWN} / (R _{UP} + R _{DOWN}) ⁽¹⁾			Without using R _{UP} or R _{DOWN}	ADCINx decoded value
MIN	Target	MAX		
0	0.0114	0.0228	tie to GND	0
0.0229	0.0475	0.0722	N/A	1
0.0723	0.1074	0.1425	N/A	2
0.1425	0.1899	0.2372	N/A	3
0.2373	0.3022	0.3671	N/A	4
0.3672	0.5368	0.7064	tie to LDO_1V5	5
0.7065	0.8062	0.9060	N/A	6
0.9061	0.9530	1.0	tie to LDO_3V3	7

(1) External resistor tolerance of 1% is recommended. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values. For convenience, the Target column shows this value.



I2C ADDR W/R 0X40/0X41



<https://realschematic.com>

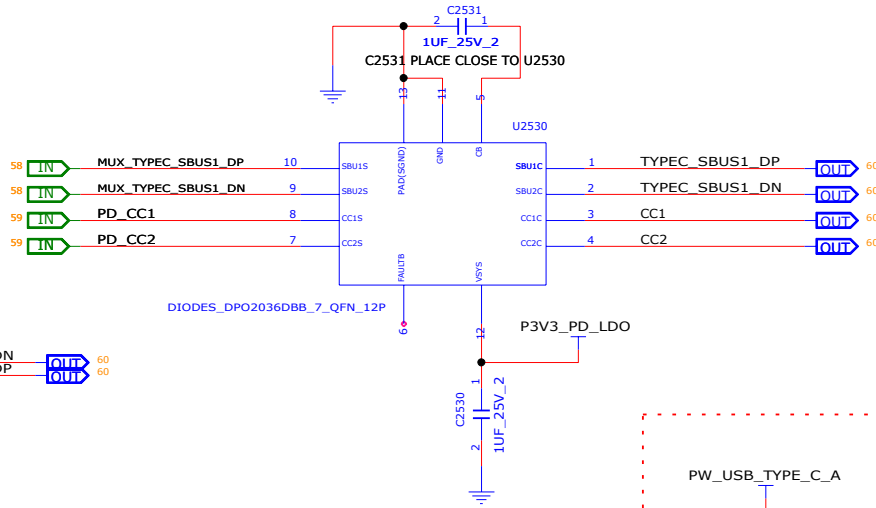
INVENTEC

TITLE: MODEL_PROJECT,FUNCTION
Block Diagram

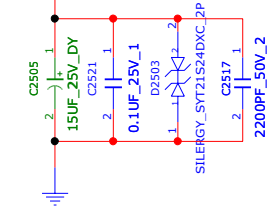
SIZE: A1 CODE: 13104XXXX-B-B REV: X01
DATE: 21-OCT-2002 PCB P/N: XXXXXXXXXXXX PCB VER: XXX SHEET: 58 of 110

TYPE C CNTR

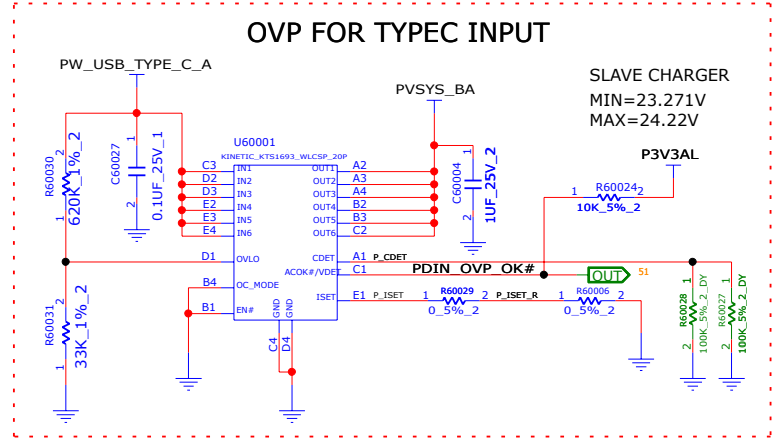
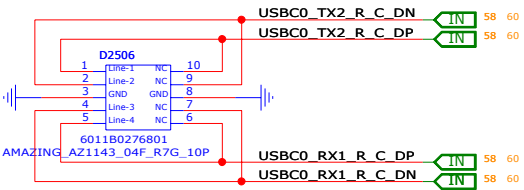
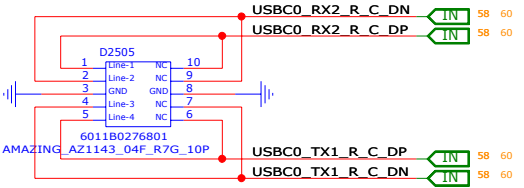
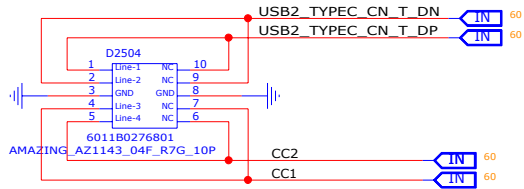
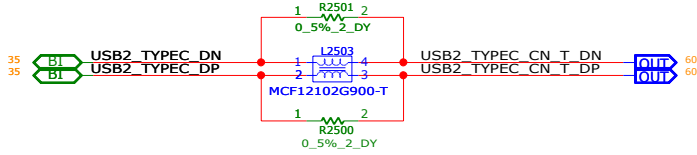
LOCATION NUMBER : 2500~2599



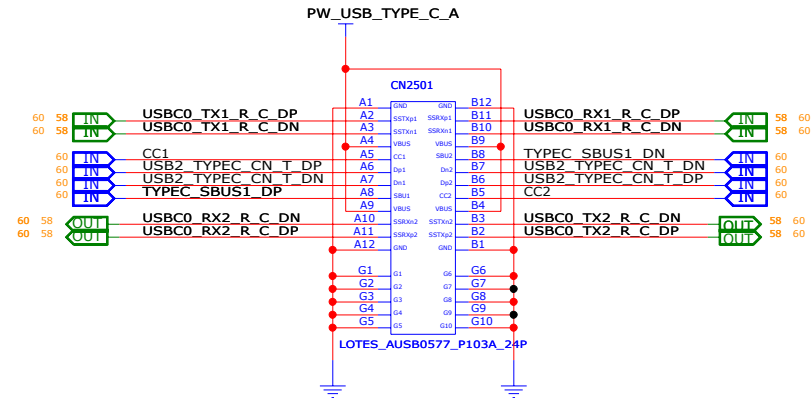
PW_USB_TYPE_C_A



RF CAPACITOR
2200PF X1



SLAVE CHARGER
MIN=23.271V
MAX=24.22V



PW_USB_TYPE_C_A

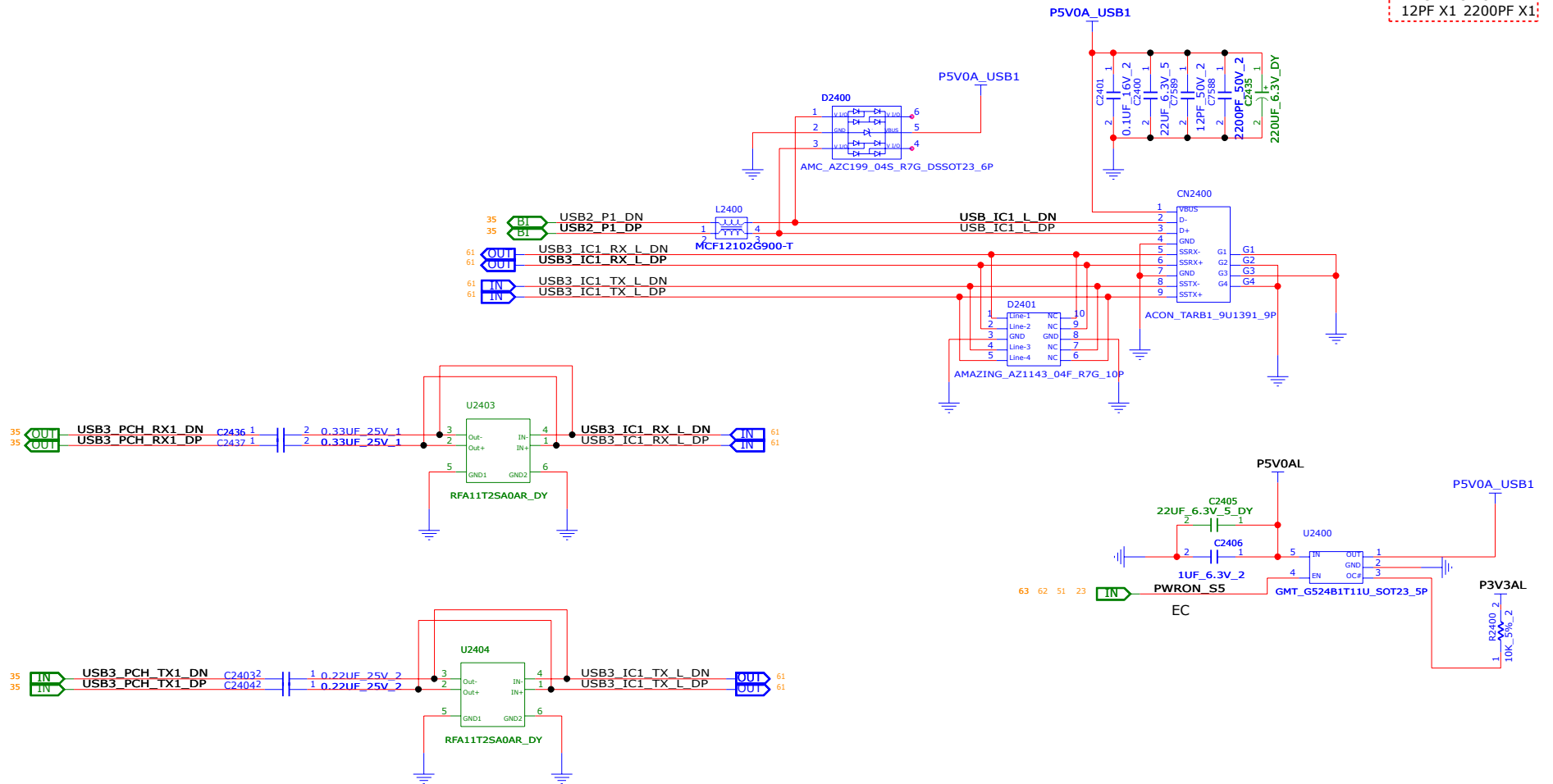
OTES_AUSB0577_P103A_24P

INVENTEC			
TITLE MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	21-OCT-2002 XXX
SHEET		60 of 119	

USB 3.0 PORT1 (LEFT SIDE)

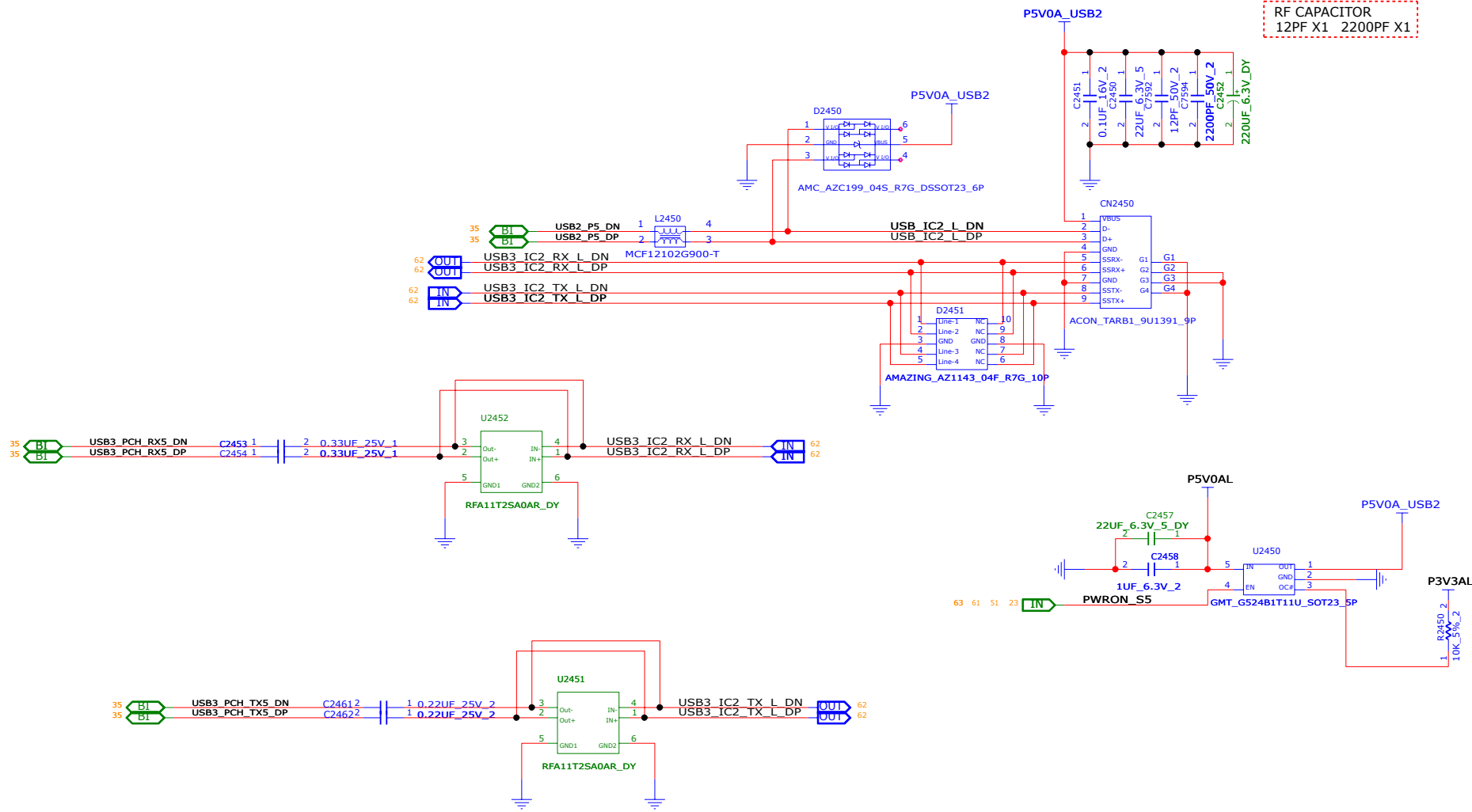
LOCATION NUMBER : 2400~2449

RF CAPACITOR
12PF X1 2200PF X1



USB 3.0 PORT2 (LEFT SIDE)

LOCATION NUMBER : 2450~2499



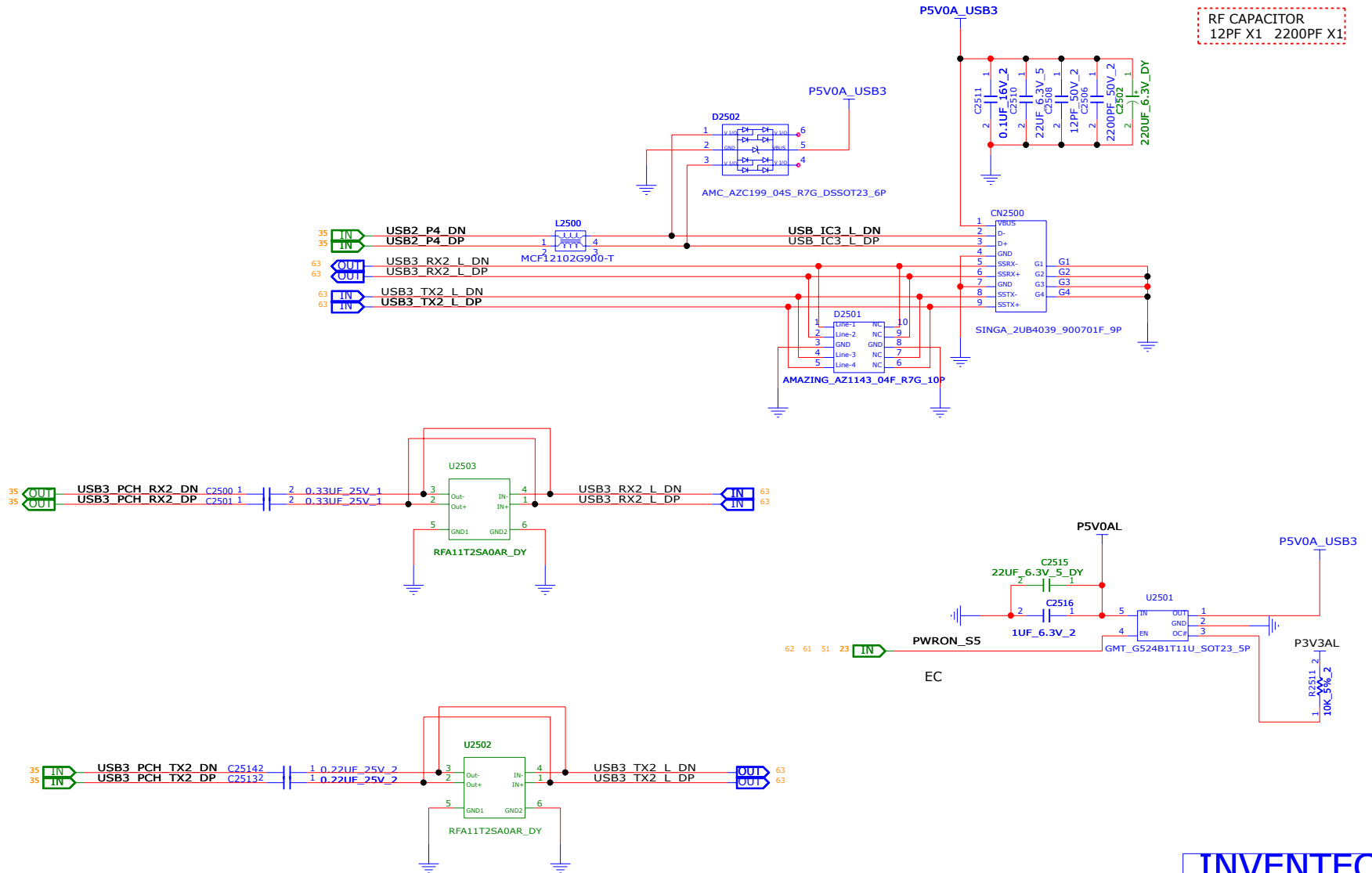
RF CAPACITOR
12PF X1 2200PF X1

INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by	DATE	PCB VER.	SHEET
XXX	21-OCT-2002	XXX	62 of 119
PCB P/N	60xxxxxxxxxxx		

<https://realschematic.com>

USB 3.0 PORT3 (REAR)

LOCATION NUMBER : 2500~2549

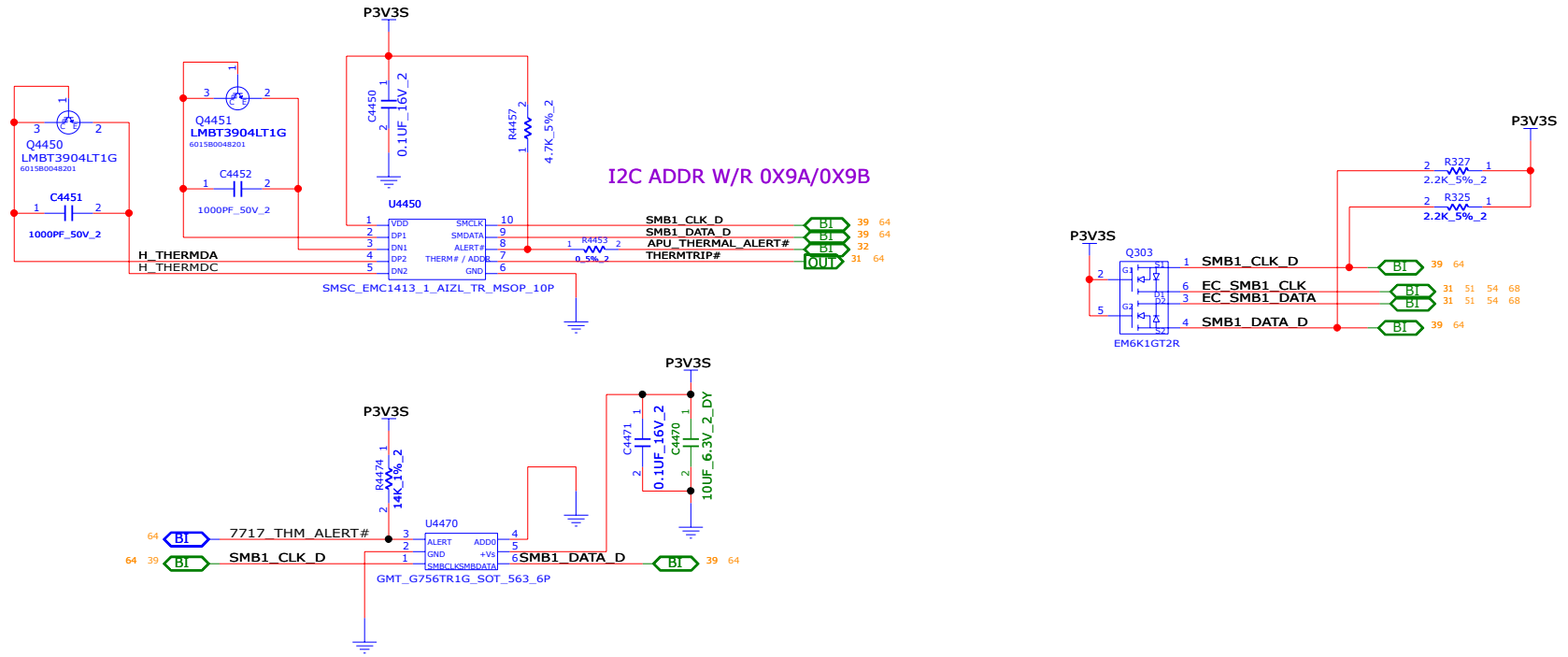


RF CAPACITOR
12PF X1 2200PF X1

INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	
PCB P/N 60xxxxxxxxxx		PCB VER XXX	
SHEET 63 of 119			

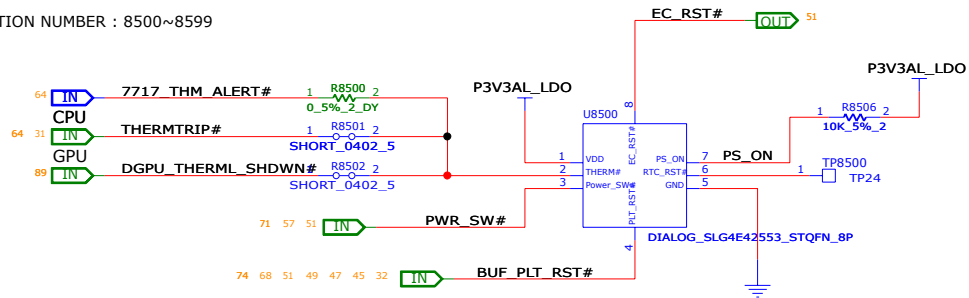
THERM SENSOR

LOCATION NUMBER: 4450~4499



EC_SHUTDOWN

LOCATION NUMBER : 8500~8599



<https://realschematic.com>

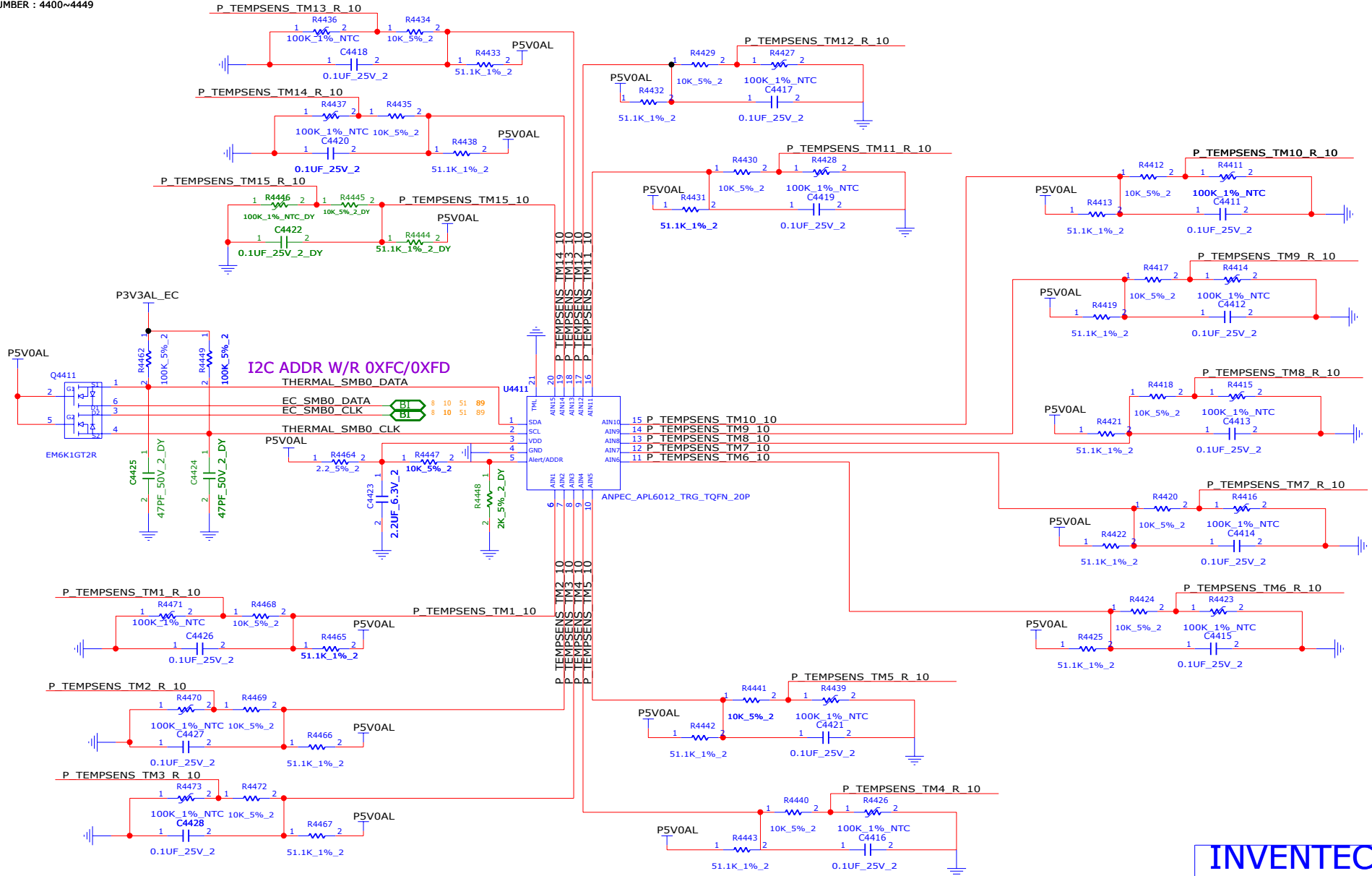
INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by		DATE	21-OCT-2002
PCB P/N		PCB VER	XXX
SHEET		64 of 119	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX
SIZE	A3	CODE	CS
SHEET		64 of 119	

THERMAL APL6012

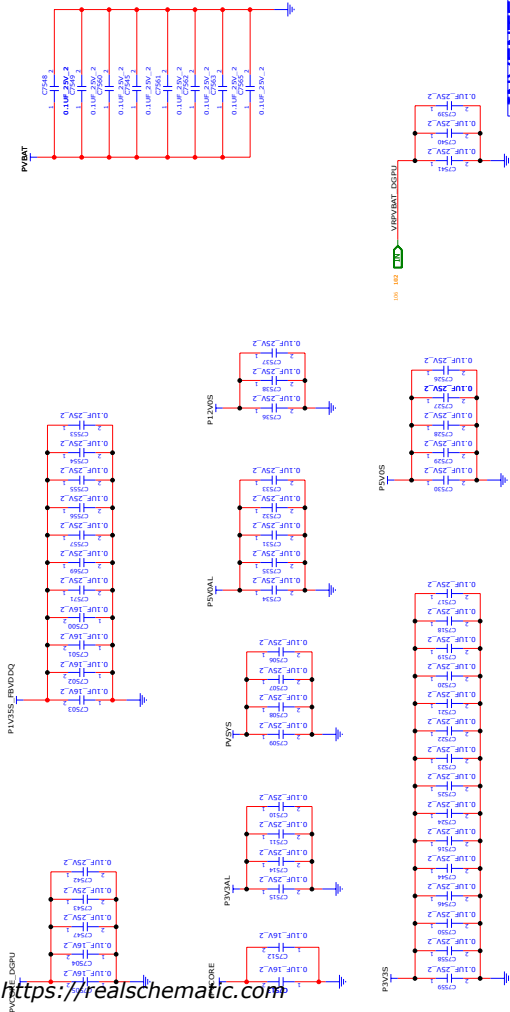
LOCATION NUMBER : 4400~4449



INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by		DATE	
PCB P/N		PCB VER	
XXX		21-OCT-2002	
60xxxxxxxxxxx		XXX	
SHEET		65 of 119	

EMI

LOCATION NUMBER: 7500-7599



<https://realschematic.com>

INVENTEC

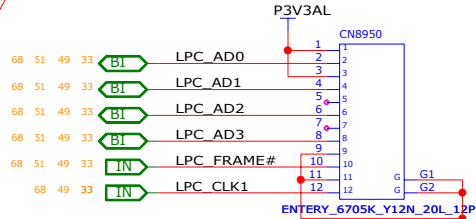
ITEM	MODEL AND SUFFIX FUNCTION	REV	NO1
DATE	DOC NUMBER	REV	NO1
DATE	DATE	DATE	DATE
DATE	DATE	DATE	DATE

DATE: 2023-12-20
DATE: 2023-12-20
DATE: 2023-12-20
DATE: 2023-12-20

DEBUG CONN

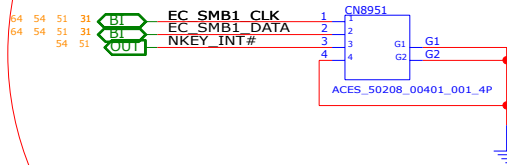
LOCATION NUMBER : 8950~8999

ASUS LPC DEBUG

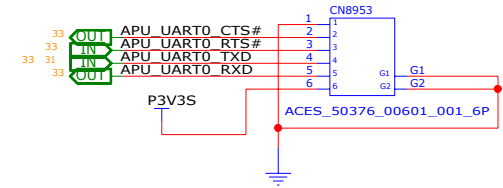


CHANGE TO ASUS CN

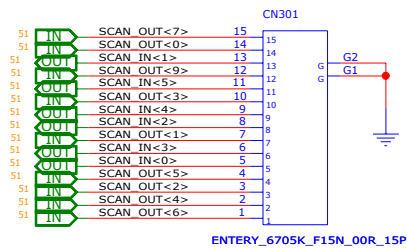
N-KEY DEBUG



CHANGE TO ASUS CN

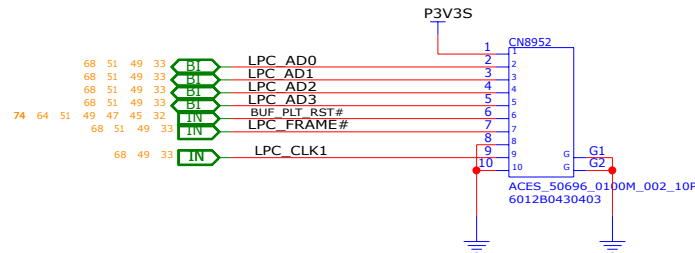


FOR ROM FLASH



CHANGE TO ASUS CN

IEC LPC DEBUG



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RESERVED

<https://realschematic.com>

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 69 of 119			

CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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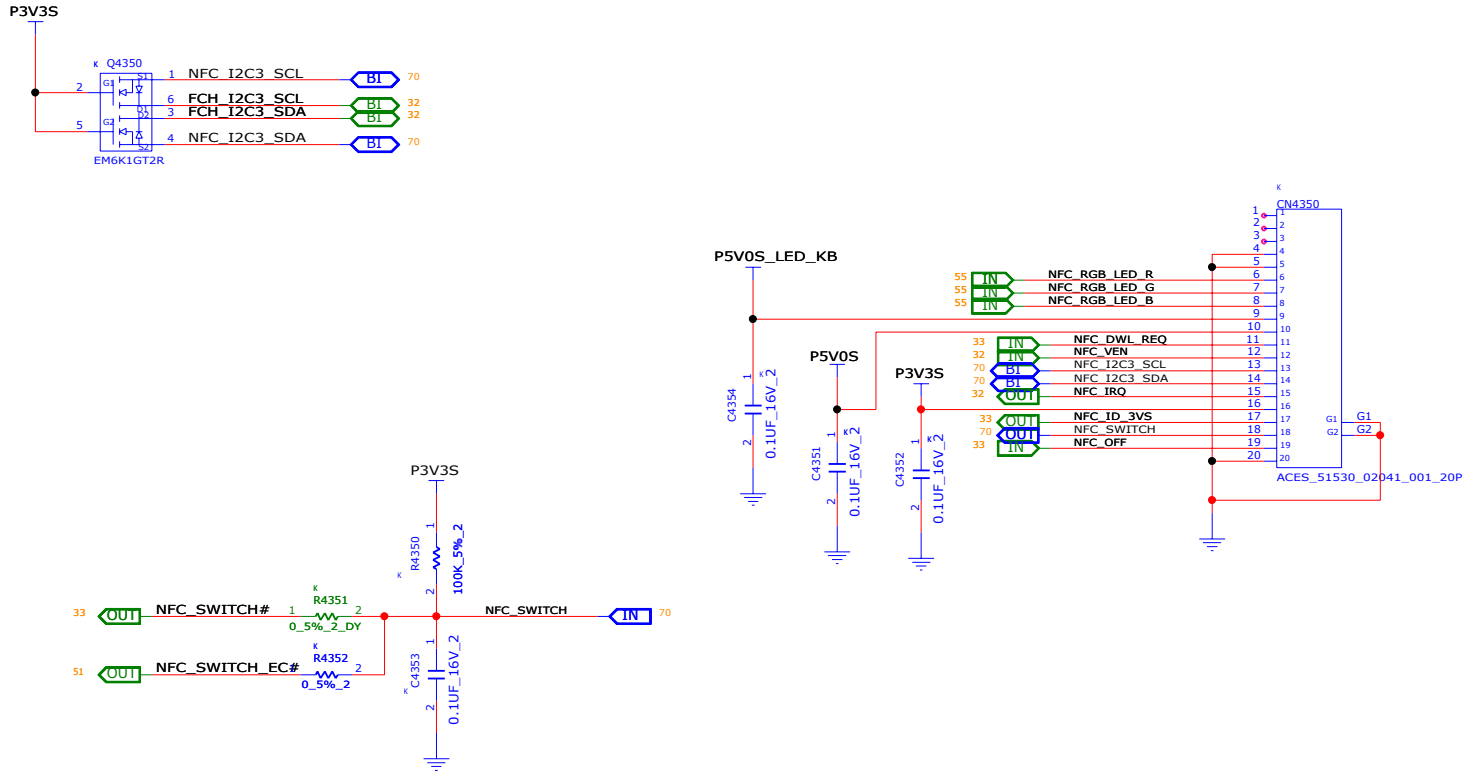
2

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MB_NFC

LOCATION NUMBER : 4350~4399

TO NFC SUB BOARD



<https://realschematic.com>

INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3 CODE CS
SHEET 70 of 119

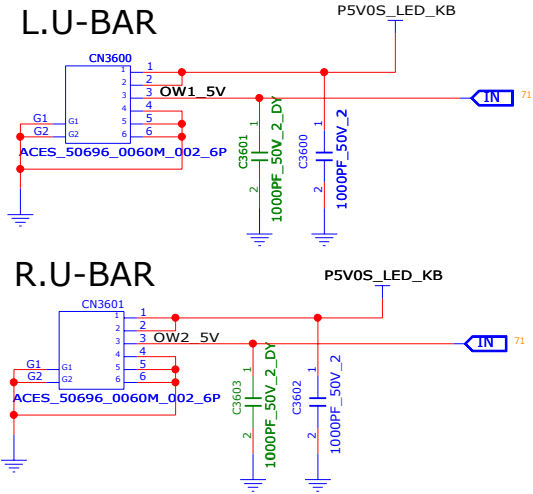
DOC. NUMBER 1310xxxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxxx PCB VER. XXX

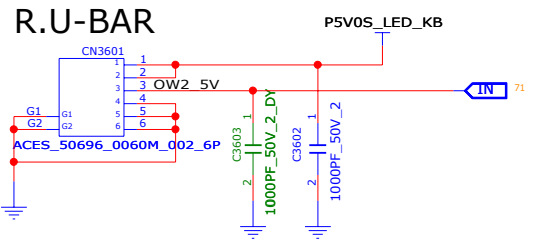
MB_L.U/R.U-BAR/INDICATOR/MIC

LOCATION NUMBER : 3500~3699

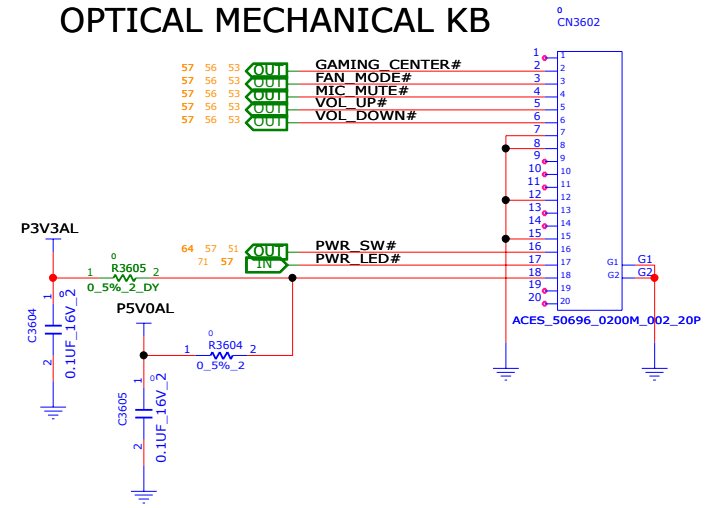
L.U-BAR



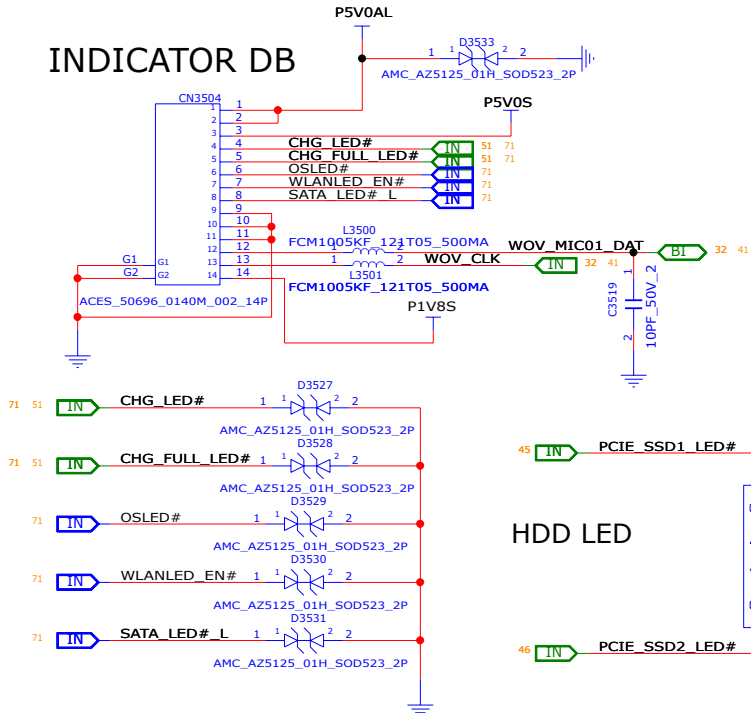
R.U-BAR



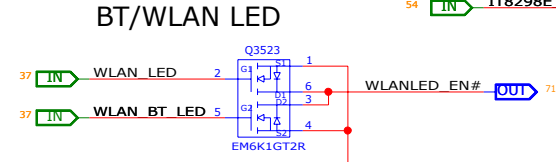
OPTICAL MECHANICAL KB



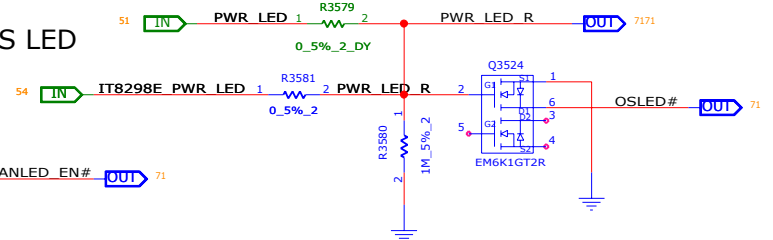
INDICATOR DB



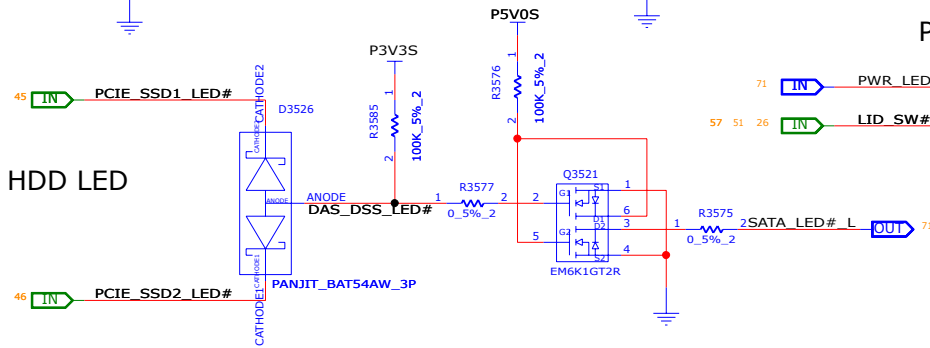
BT/WLAN LED



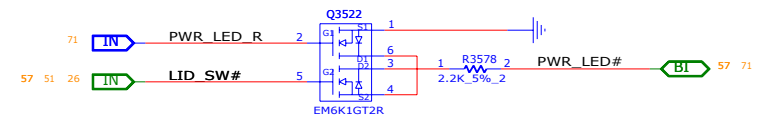
OS LED



HDD LED



POWER KEY LED



INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET		71	of 119

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

GN20 E7

8GB GDDR6 256M X 16 X 2 X6

INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
SHEET		72 of 119	

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<https://realschematic.com>

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	SHEET
XXX 60xxxxxxxxxx		21-OCT-2002 XXX	73 of 119

8

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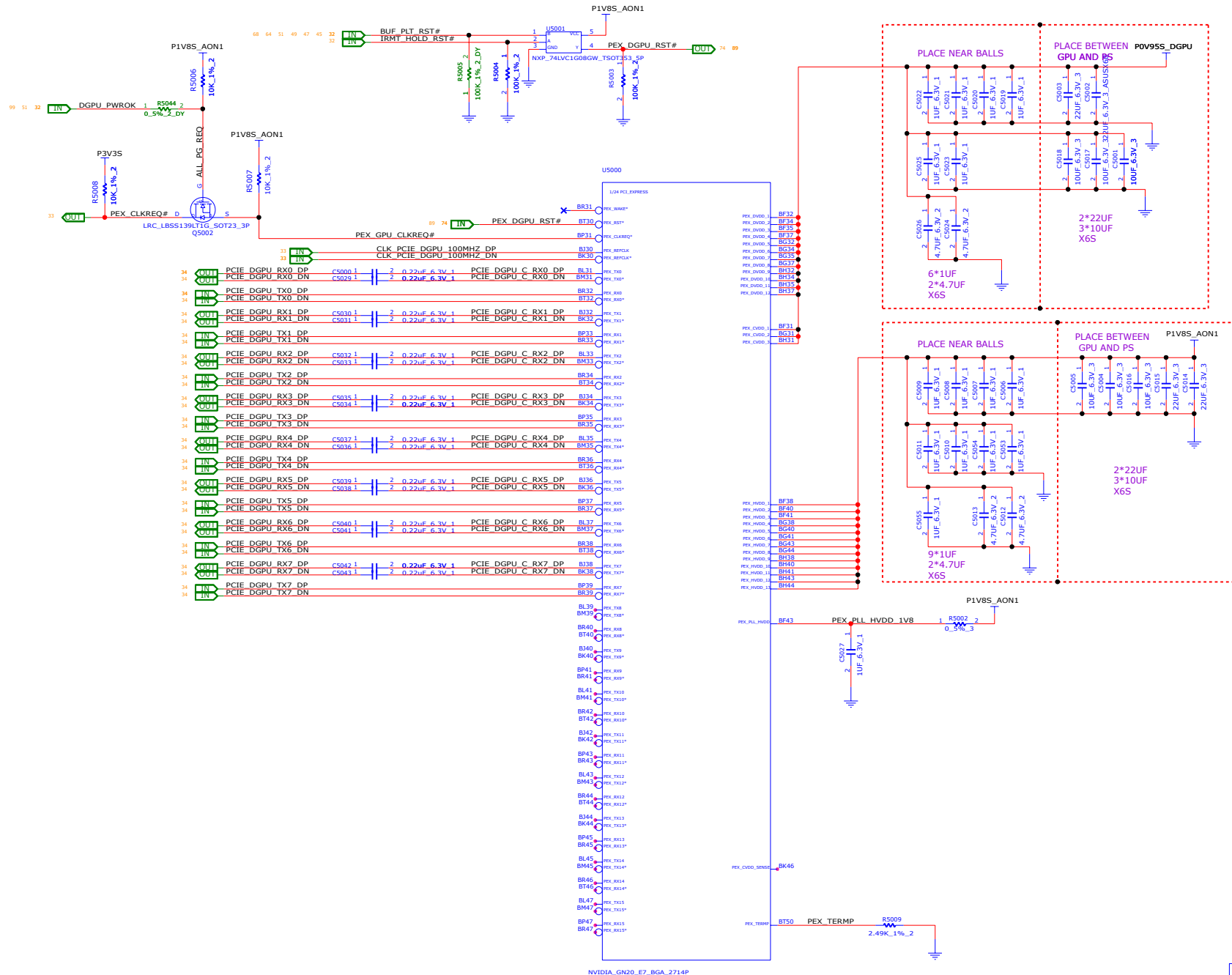
3

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GPU PCI EXPRESS

LOCATION NUMBER : 5000~5499



<https://realschematic.com>

INVENTEC

TITLE	MODEL_PROJECT_FUNCTION	DOC NUMBER	REV
Block Diagram		1310xxxxx-0-B	X01
CHANGE BY	DATE	21-OCT-2002	
PCB P/N	PCB VER	XXX	
SIZE	CODE	SHEET	1 of 110

GPU MEMORY PARTITION A

LOCATION NUMBER : 5000~5499

U5000

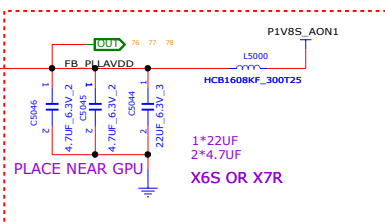
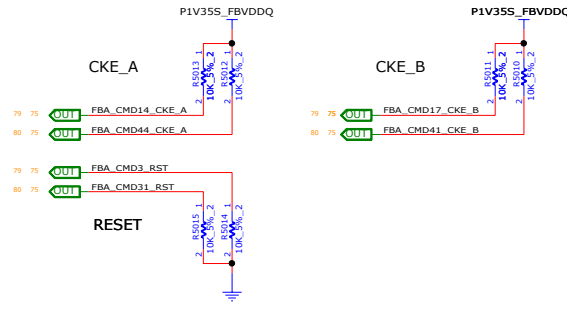
NVIDIA_GN20_E7_BGA_2714P



Page29: MISC: ROM, Straps

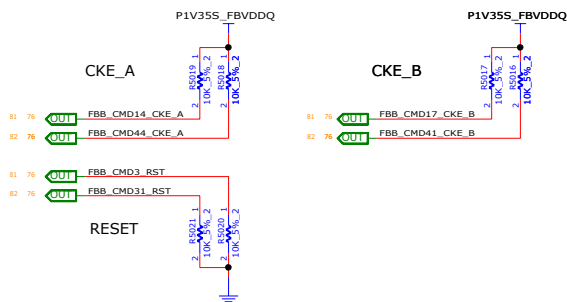
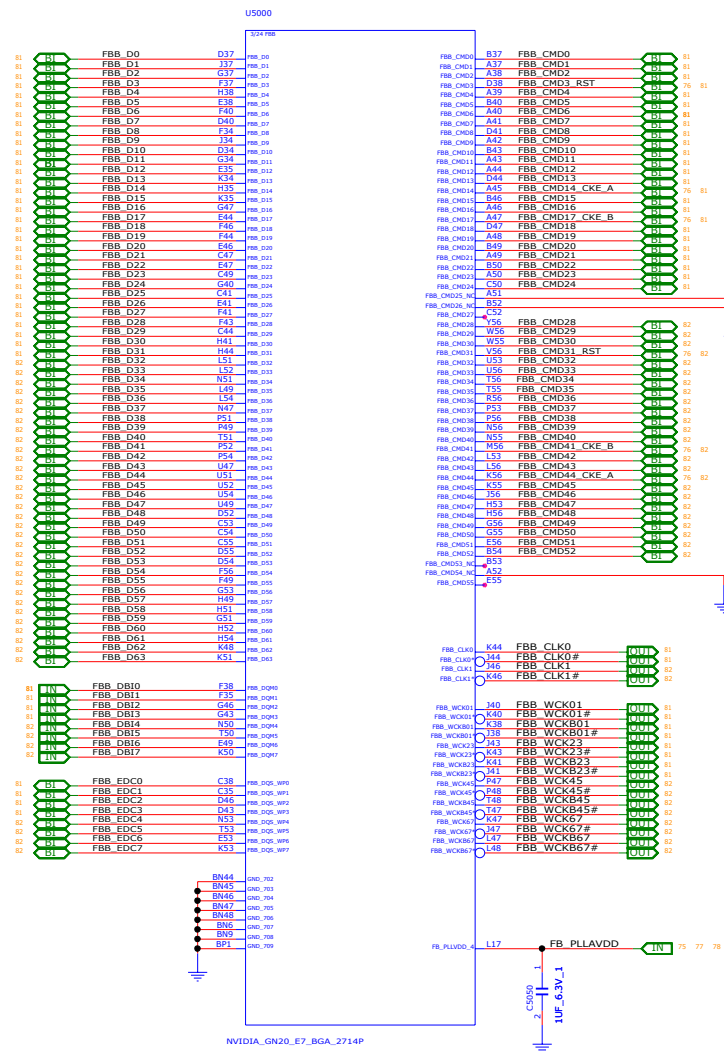
STRAP	STRAP	STRAP	STRAP	STRAP	STRAP	STRAP	STRAP	STRAP	STRAP
L	L	L	0000	MARKED TO					
L	R	L	0000	MARKED TO					
L	R	R	0000	MARKED TO					DEFAULT
L	R	L	0000	MARKED TO					
L	L	R	0000	MARKED TO					

STRAP	STRAP	STRAP	STRAP	STRAP	STRAP	STRAP	STRAP	STRAP	STRAP
L	R	R	1	1	1	1	1	1	1
R	R	L	1	1	1	1	1	1	1
R	L	L	1	1	1	1	1	1	1
R	L	L	1	1	1	1	1	1	1
L	L	R	1	1	1	1	1	1	1



GPU MEMORY PARTITION B

LOCATION NUMBER : 5000~5499



NVIDIA_GN20_E7_BGA_2714P

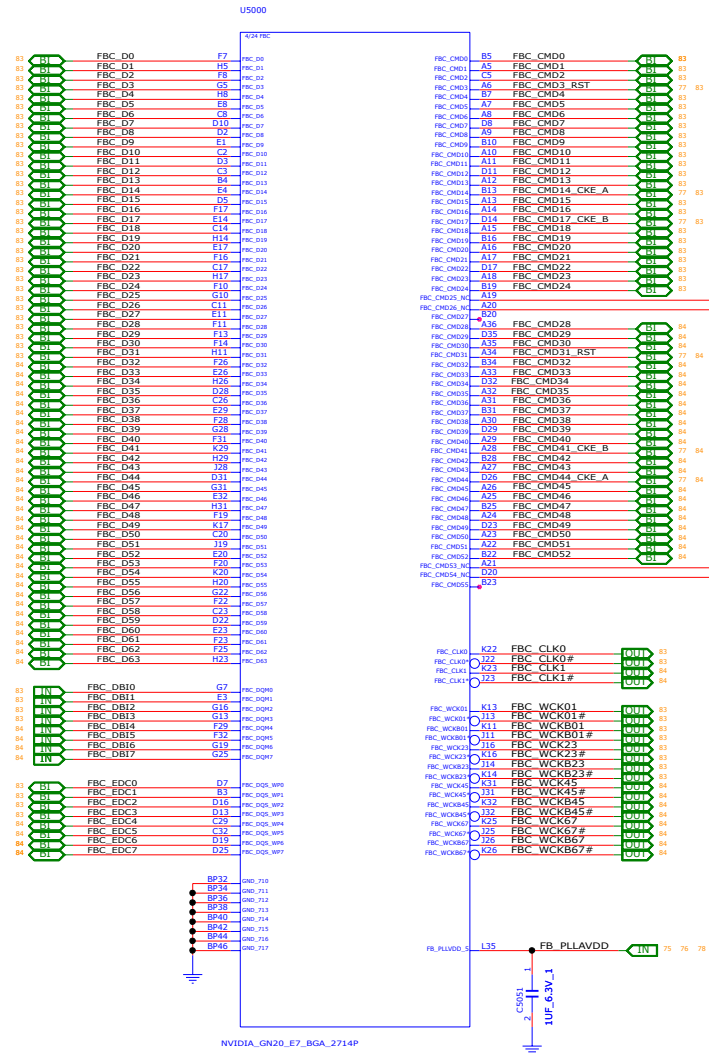
<https://realschematic.com>

INVENTEC

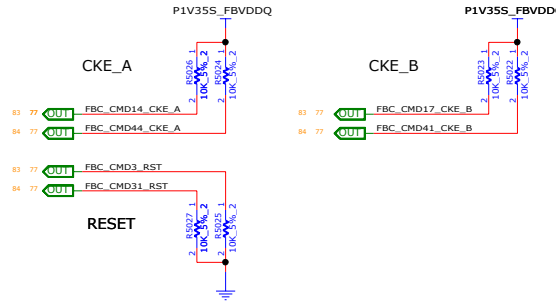
TITLE	MODEL_PROJECT,FUNCTION	DOC,NUMBER	REV
Block	Diagram	1310xxxxx-B-B	X01
SIZE	A1	CS	76 of 116
CHANGE IN	XXX	DATE	21-OCT-2002
P/CB P/N	6Pxxxxxxxxxx	P/CB VER	XXX

GPU MEMORY PARTITION C

LOCATION NUMBER : 5000~5499



GAIXX GDDR6 CMD Mapping		x16 Mode	
Lower 0..31 DRAM1 CHA-Byte 0,1		Upper 32..63 DRAM2 CHB-Byte 4,5	
CA0_A	CMD1	CMD33	CMD33
CA1_A	CMD13	CMD45	CMD35
CA2_A	CMD12	CMD35	CMD35
CA3_A	CMD24	CMD46	CMD36
CA4_A	CMD11	CMD36	CMD36
CA5_A	CMD15	CMD43	CMD37
CA6_A	CMD22	CMD48	CMD38
CA7_A	CMD23	CMD47	CMD39
CA8_A	CMD0	CMD34	CMD40
CA9_A	CMD2	CMD32	CMD41
CAB_A	CMD10	CMD37	CMD42
CKE_A	CMD14	CMD44	CMD43
CA0_B	CMD5	CMD29	CMD44
CA1_B	CMD18	CMD52	CMD45
CA2_B	CMD7	CMD40	CMD46
CA3_B	CMD20	CMD50	CMD47
CA4_B	CMD8	CMD39	CMD48
CA5_B	CMD16	CMD42	CMD49
CA6_B	CMD21	CMD49	CMD50
CA7_B	CMD19	CMD51	CMD51
CA8_B	CMD6	CMD28	CMD52
CA9_B	CMD4	CMD30	CMD53
CAB_B	CMD9	CMD38	CMD54
CKE_B	CMD17	CMD41	CMD55
RESET*	CMD3	CMD31	



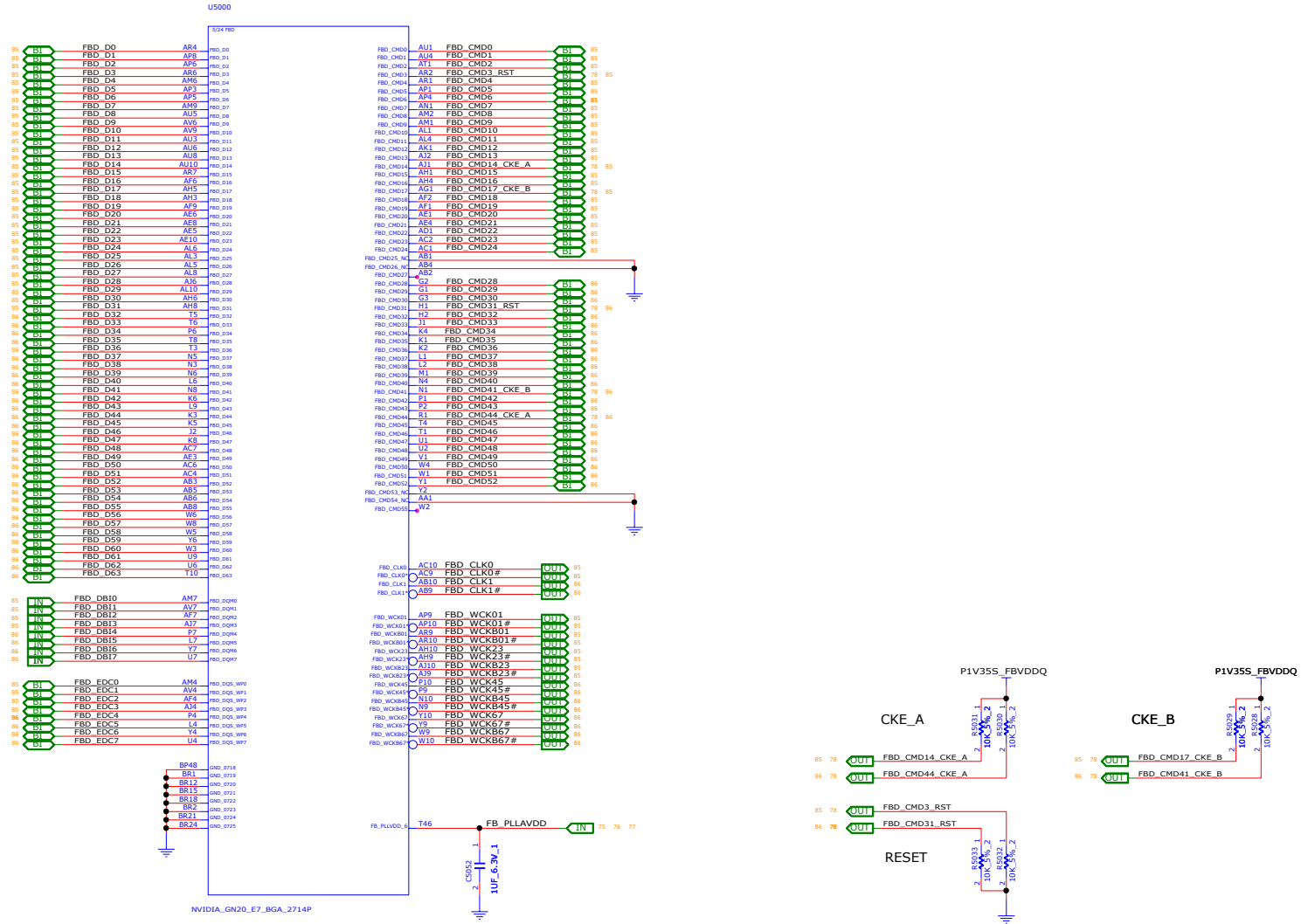
<https://realschematic.com>

INVENTEC

TITLE	MODEL_PROJECT,FUNCTION	REV
Block	Diagram	X01
DOC NUMBER	1310xxxxx-0-B	
CHANGE BY	DATE	21-OCT-2002
P/CB P/N	P/CB VER	XXX
SIZE A1	SHEET	77 of 110

GPU MEMORY PARTITION D

LOCATION NUMBER : 5000~5499



INVENTEC

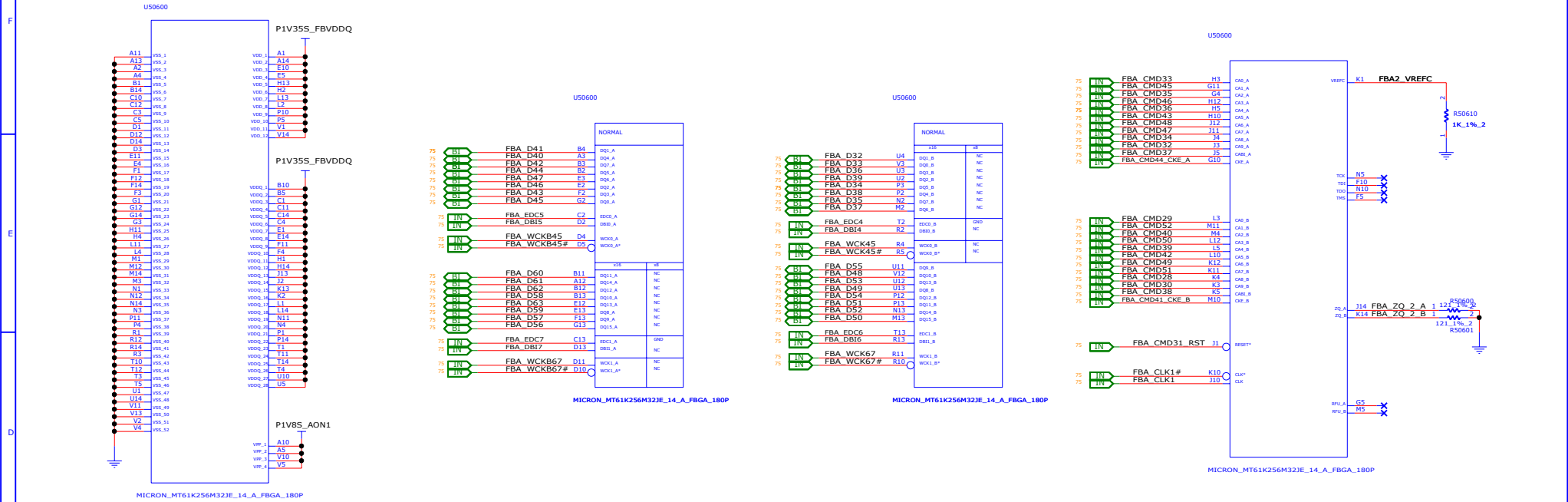
MODEL PROJECT FUNCTION

1310xxxxx-B-B

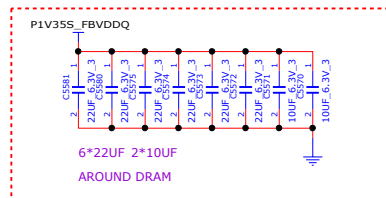
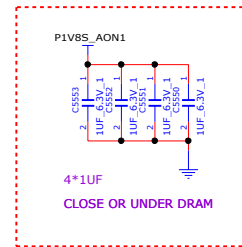
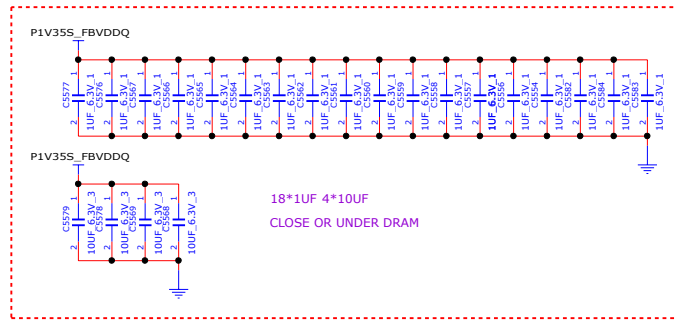
CHANGE I#	XXX	DATE	21-OCT-2002	SIZE	CODE	DOC NUMBER	REV
P/CB P/N	6Pxxxxxxxxxx	P/CB VER	XXX	SHEET	76	of	110

GPU MEMORY FBA PARTITION 63-32

LOCATION NUMBER : 5550~5599



DECAP VIA : AT LEAST 2 GND VIAS AND 2 POWER VIAS FOR EACH CAP



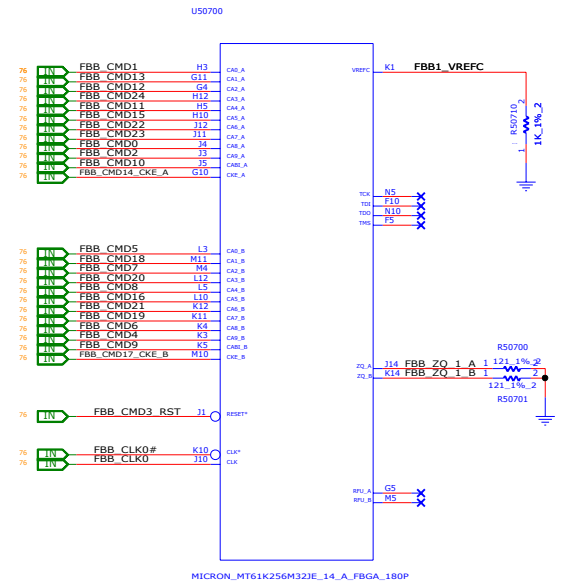
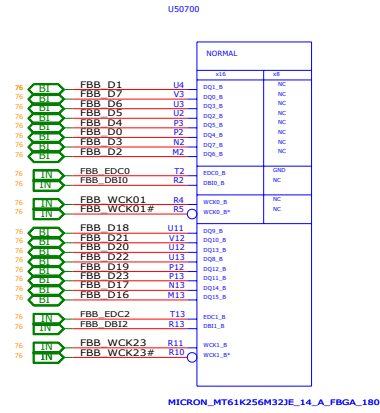
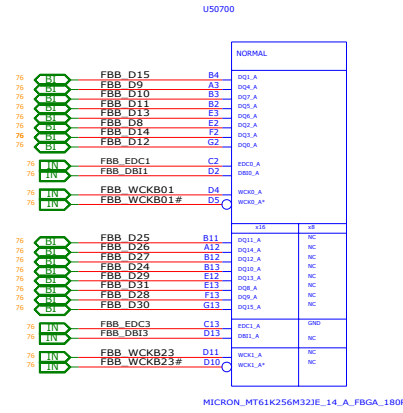
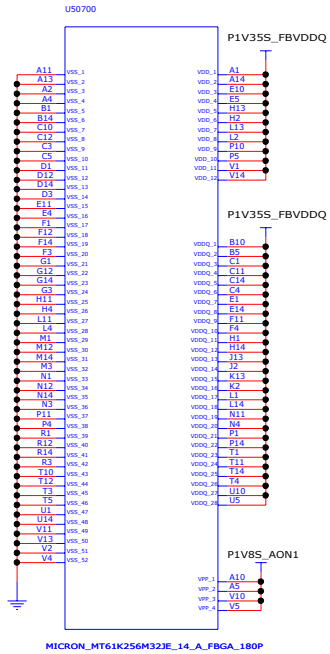
<https://realschematic.com>

INVENTEC

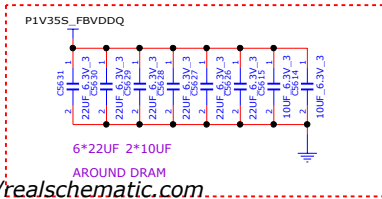
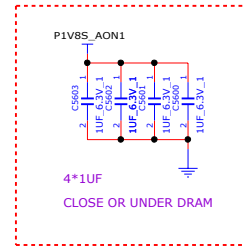
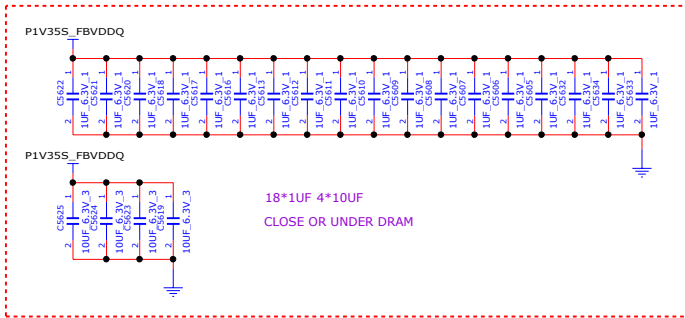
TITLE	MODEL,PROJECT,FUNCTION	REV
Block	Diagram	X01
CHANGE IN	DATE	13104XXXX-B-B
P/CB P/N	P/CB VER	80 of 110

GPU MEMORY FBB PARTITION 31-0

LOCATION NUMBER : 5600~5649



DECAP VIA : AT LEAST 2 GND VIAS AND 2 POWER VIAS FOR EACH CAP



<https://realschematic.com>

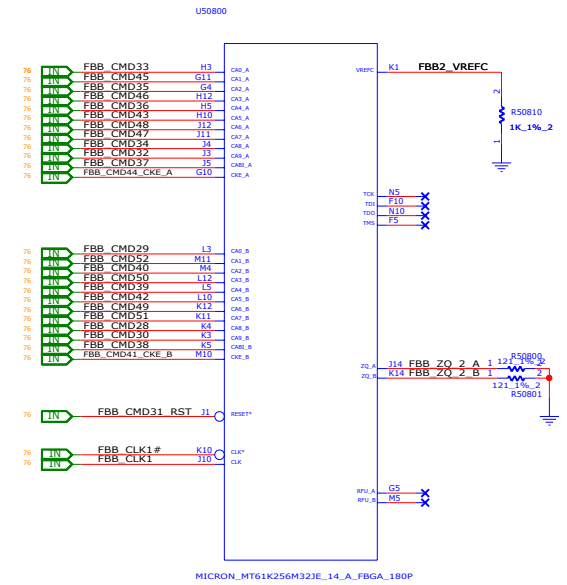
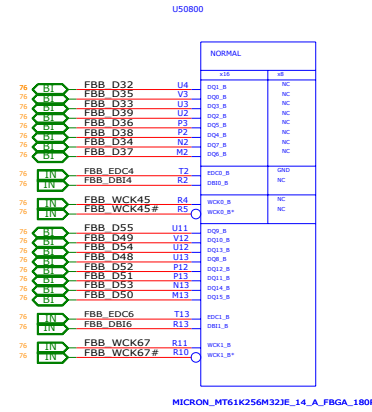
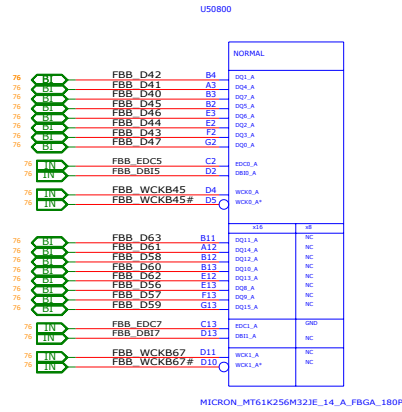
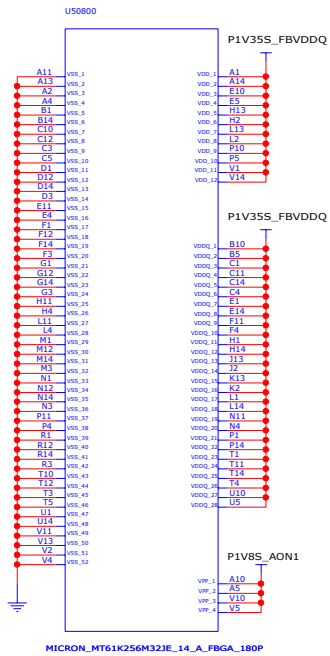
INVENTEC

TITLE	MODEL_PROJECT,FUNCTION	DOC NUMBER	REV
Block	Diagram	1310xxxx-B-B	X01
SIZE	CODE	REV	
A1	CS	11	110

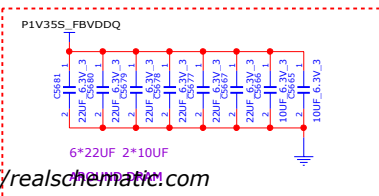
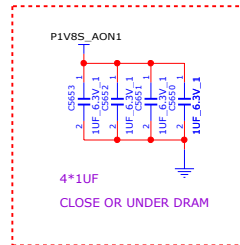
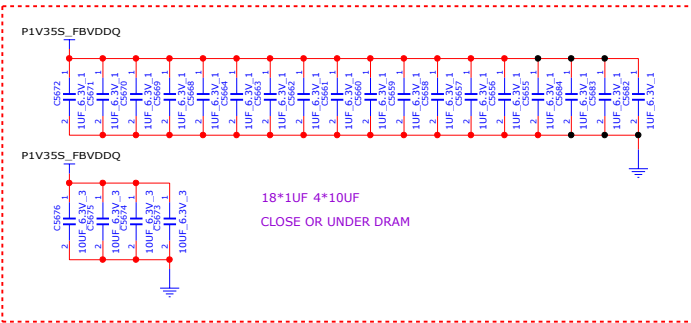
CHANGE IN	XXX	DATE	21-OCT-2002
P/CB P/N	6Pxxxxxxxxxx	P/CB VER	XXX

GPU MEMORY FBB PARTITION 63-32

LOCATION NUMBER : 5650-5699



DECAP VIA : AT LEAST 2 GND VIAS AND 2 POWER VIAS FOR EACH CAP



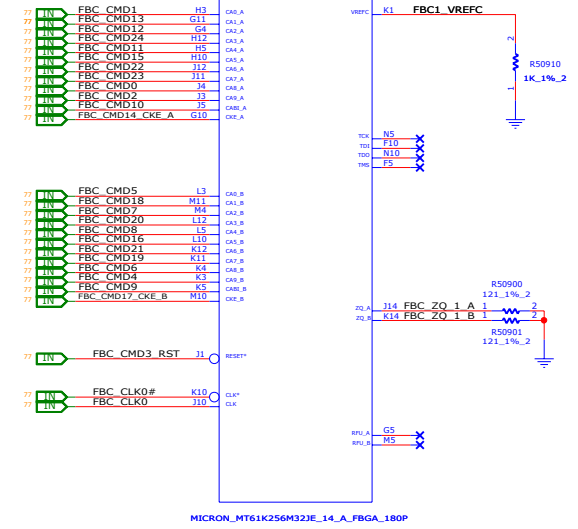
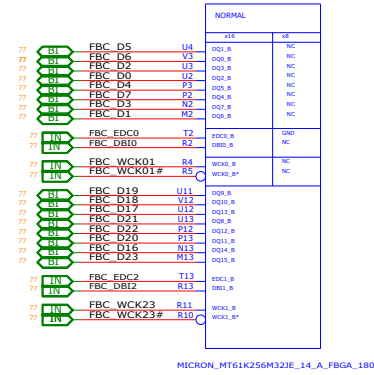
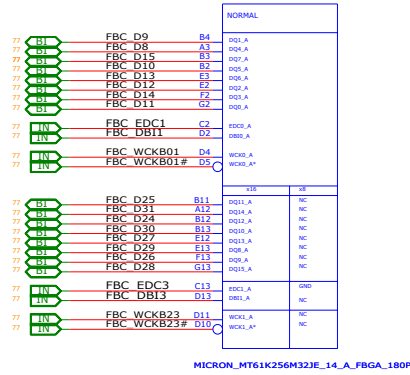
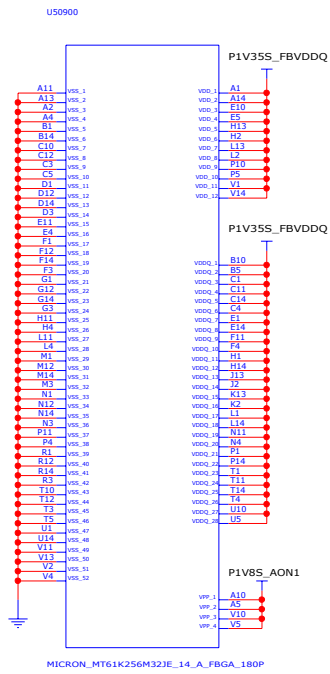
<https://realschematic.com>

INVENTEC

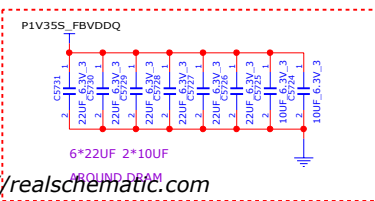
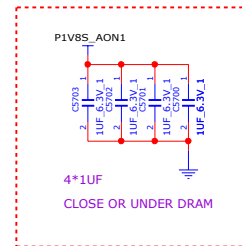
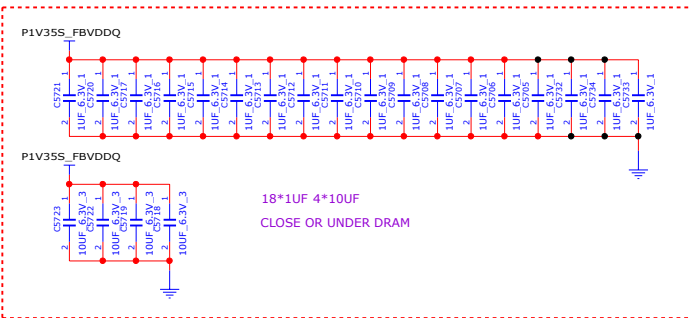
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Block	Diagram	13104xxxx-B-B	X01
SIZE	A1	CS	110
CHANGE IN	XXX	DATE	21-OCT-2002
P/CB P/N	6Pxxxxxxxxxxxx	P/CB VER	XXX
SHEET	31	OF	110

GPU MEMORY FBC PARTITION 31-0

LOCATION NUMBER : 5700~5749



DECAP VIA : AT LEAST 2 GND VIAS AND 2 POWER VIAS FOR EACH CAP



<https://realschematic.com>

INVENTEC

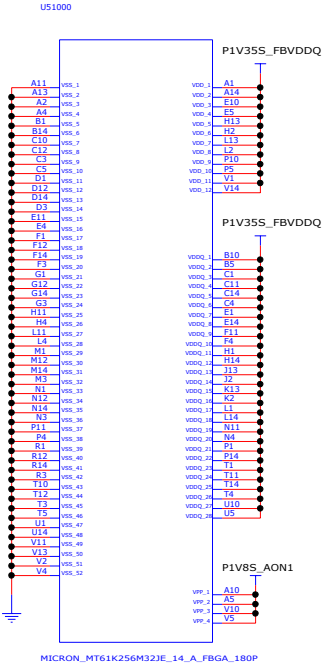
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE: A1 CODE: 13104XXXX-B-B REV: X01
CS: SHEET: 81 of 110

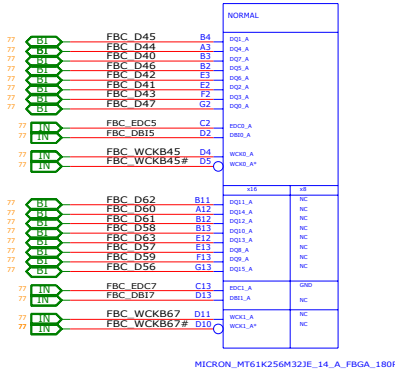
CHANGE BY: XXXX DATE: 21-OCT-2002
PCB P/N: 6PXXXXXXXXXX PCB VER: XXXX

GPU MEMORY FBC PARTITION 63-32

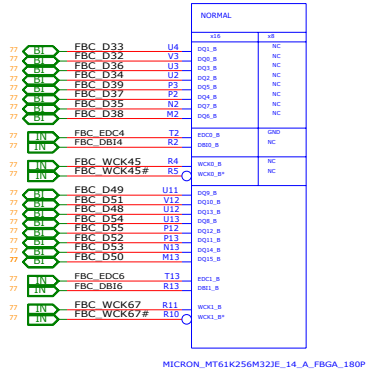
LOCATION NUMBER : 5750~5799



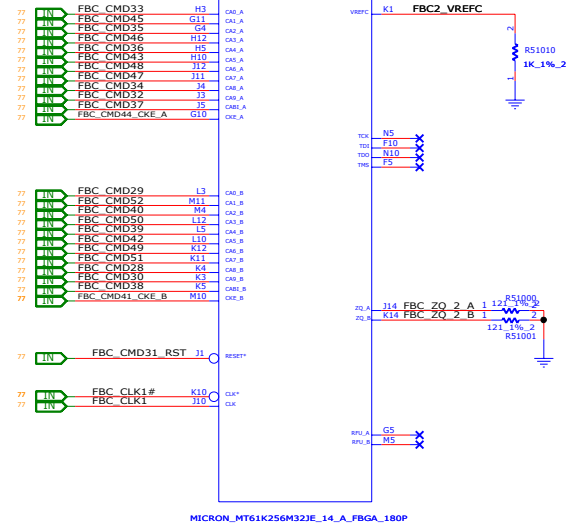
MICRON_MT61K256M32JE_14_A_FBGA_180P



MICRON_MT61K256M32JE_14_A_FBGA_180P

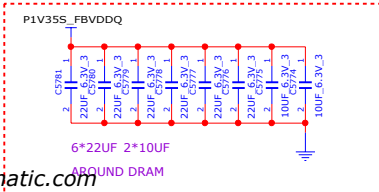
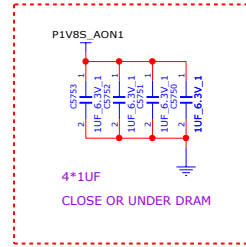
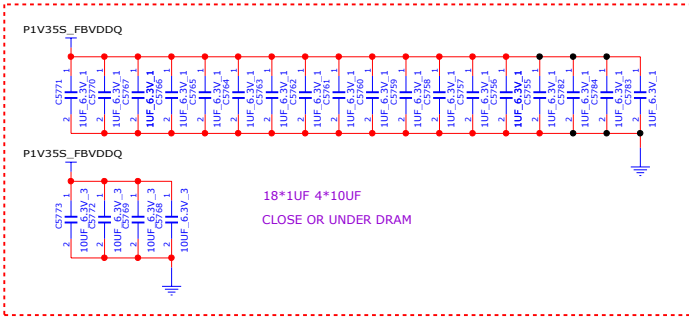


MICRON_MT61K256M32JE_14_A_FBGA_180P



MICRON_MT61K256M32JE_14_A_FBGA_180P

DECAP VIA : AT LEAST 2 GND VIAS AND 2 POWER VIAS FOR EACH CAP

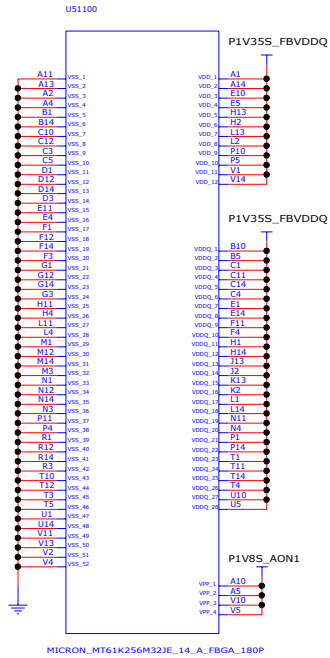


<https://realschematic.com>

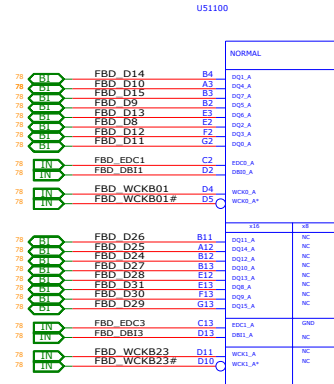
INVENTEC			
TITLE			
Block		Diagram	
MODEL_PROJECT_FUNCTION			
SIZE	CODE	DOC NUMBER	REV
A1	CS	13104xxxx-B-B	X01
SHEET 34 of 110			

GPU MEMORY FBD PARTITION 31-0

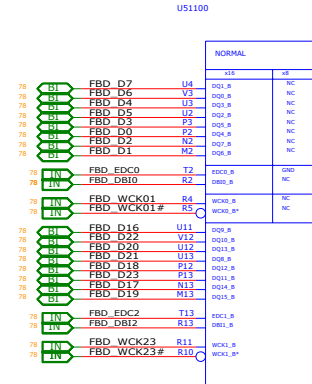
LOCATION NUMBER : 5800~5849



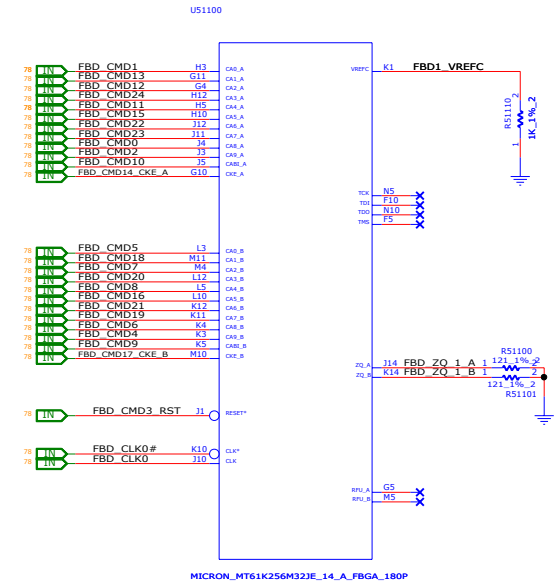
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MICRON_MT61K256M32JE_14_A_FBGA_180P

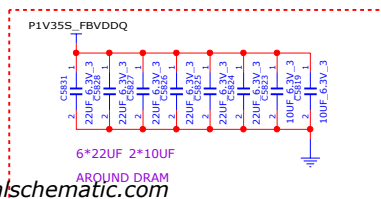
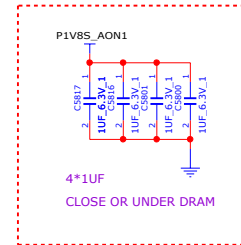
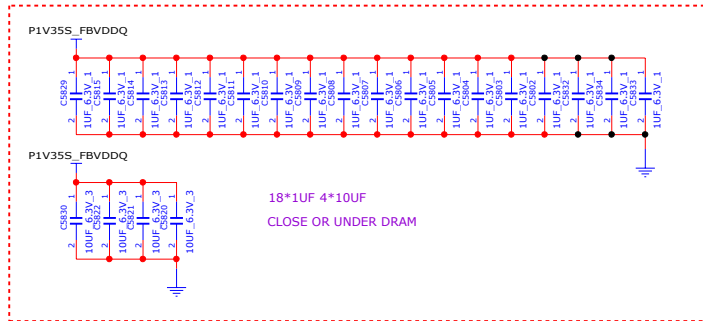


MICRON_MT61K256M32JE_14_A_FBGA_180P



MICRON_MT61K256M32JE_14_A_FBGA_180P

DECAP VIA : AT LEAST 2 GND VIAS AND 2 POWER VIAS FOR EACH CAP



<https://realschematic.com>

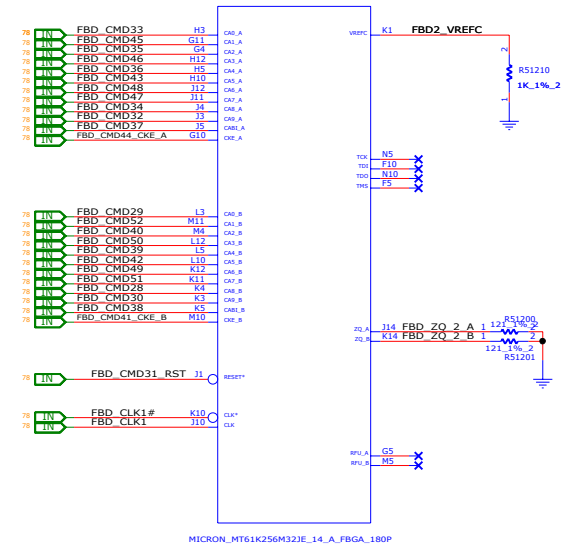
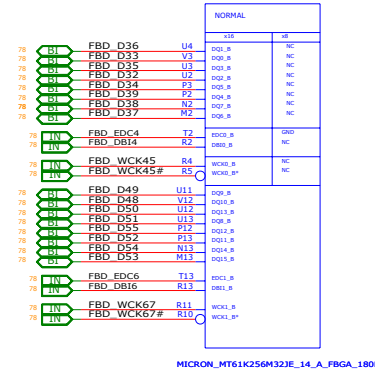
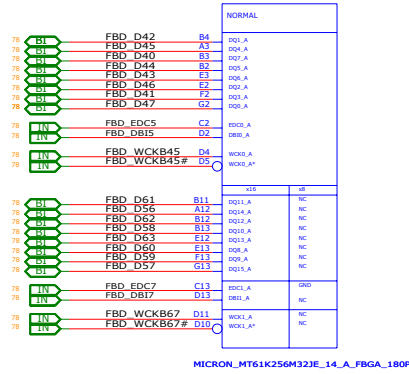
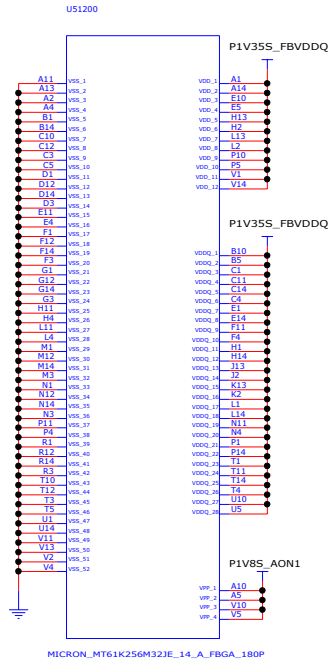
INVENTEC

TITLE	MODEL,PROJECT,FUNCTION	REV
Block	Diagram	X01
SIZE	CODE	DOC NUMBER
A1	CS	13104xxxx-B-B
SHEET	85	OF 110

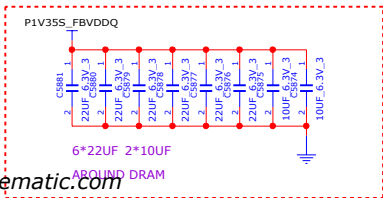
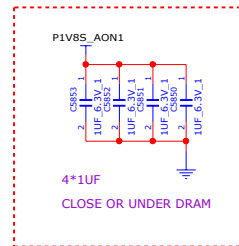
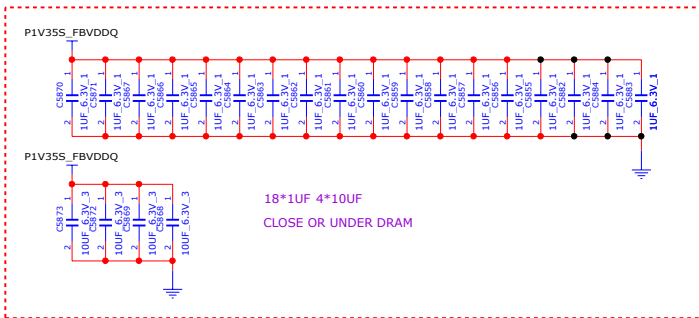
CHANGE BY	XXX	DATE	21-OCT-2002
P/CB P/N	6Pxxxxxxxxxxxx	P/CB VER	XXX

GPU MEMORY FBD PARTITION 63-32

LOCATION NUMBER : 5850~5899



DECAP VIA : AT LEAST 2 GND VIAS AND 2 POWER VIAS FOR EACH CAP



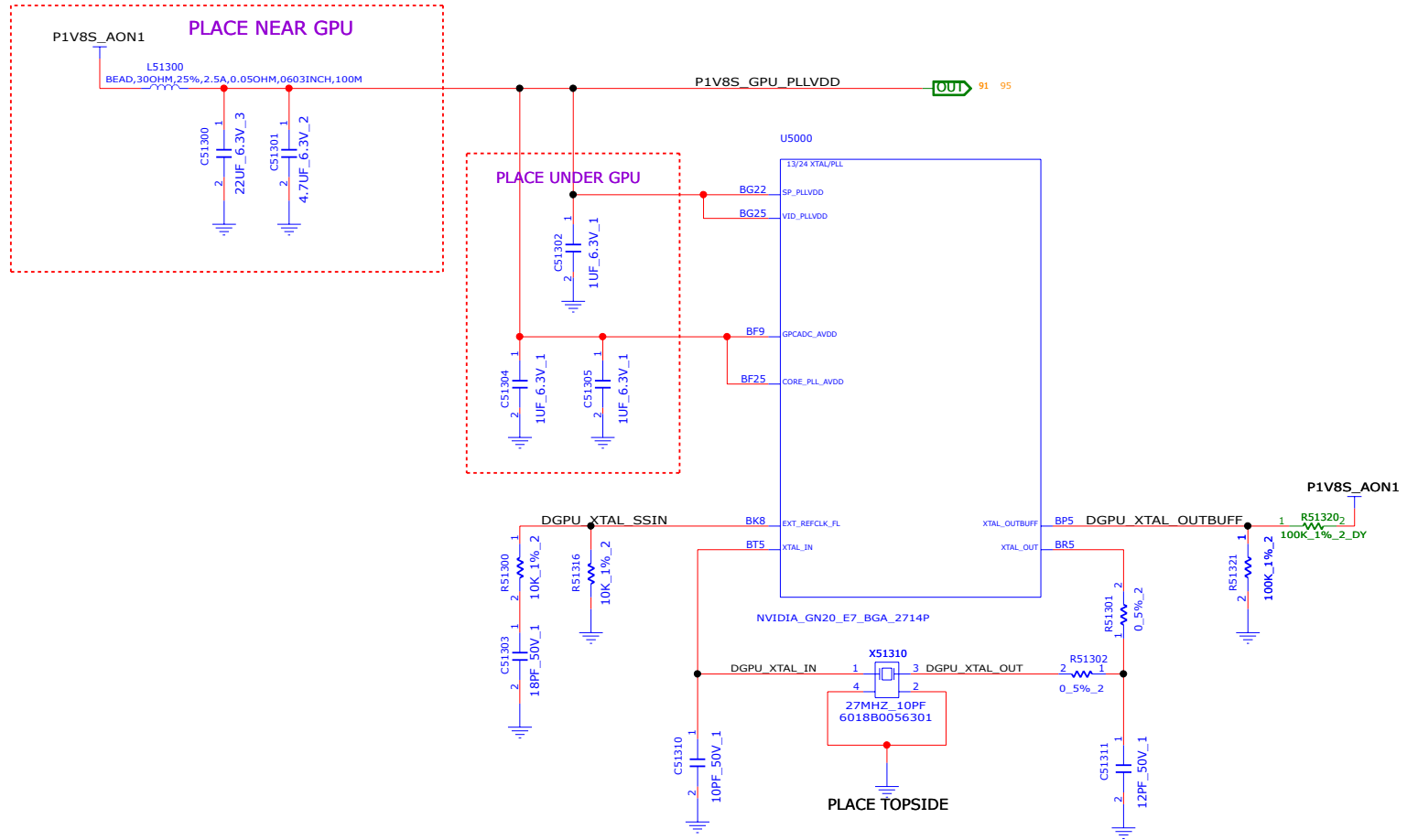
<https://realschematic.com>

INVENTEC

TITLE	MODEL_PROJECT,FUNCTION	SIZE	CODE	DOC NUMBER	REV
Block	Diagram	A1	CS	1310Axxxx-B-B	X01
CHANGE IN	XXX	DATE	21-OCT-2002		
P/CB P/N	6Pxxxxxxxxxx	P/CB VER	XXX		
		SHEET	36	of	110

GPU 27 MHZ XTAL

LOCATION NUMBER : 5000~5499, 51300~51399



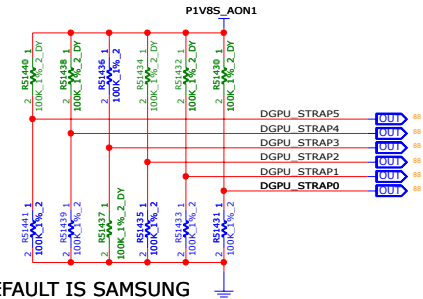
<https://realschematic.com>

INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by		DATE	
PCB P/N		PCB VER	
XXX		21-OCT-2002	XXX
SHEET		87 of 119	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX

GPU VBIOS, STRAPS

LOCATION NUMBER : 5000~5499, 51400~51499



DEFAULT IS SAMSUNG

SAMSUNG K4Z80325BC-HC14 MICRON MT61K256M32JE-14:A
 6019B2086501 6019B1847701
 STRAP 0X0=000 STRAP 0X1=001
 SAMSUNG K4ZAF325BM-HC14 MICRON :R51430 STUFF
 6019B2086601 R51431 NOT STUFF
 STRAP 0X9=0M0

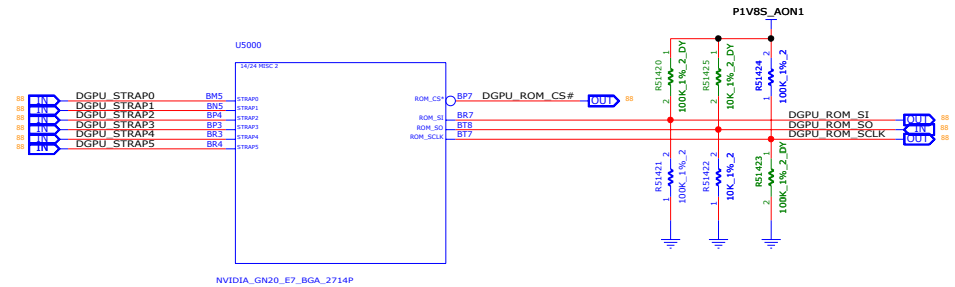
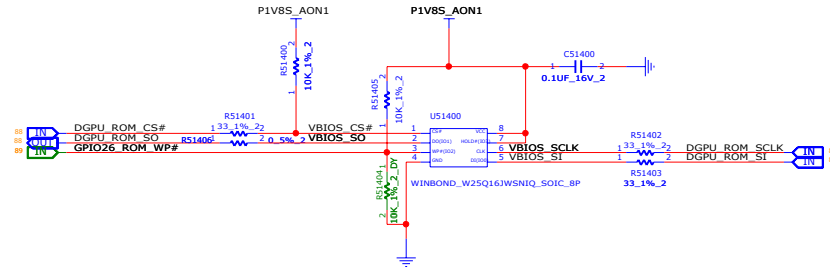


Table 9.3 RAMCFG

Strap Pins see Note	RAMCFG Setting Number
STRAP2 STRAP1 STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L L L	0 (0x0000)
L L H	1 (0x0001)
L H L	2 (0x0002)
L H H	3 (0x0003)
H L L	4 (0x0004)
H L H	5 (0x0005)
H H L	6 (0x0006)
H H H	7 (0x0007)
L L M	8 (0x0008)
L M L	9 (0x0009)
L M M	10 (0x000A)
L H M	11 (0x000B)
M L L	12 (0x000C)
M L H	13 (0x000D)
M H L	14 (0x000E)
M H H	15 (0x000F)

Strap Pins see Note	RAMCFG Setting Number
STRAP2 STRAP1 STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
H L M	16 (0x0010)
H M L	17 (0x0011)
H M H	18 (0x0012)
H H M	19 (0x0013)
L M M	20 (0x0014)
M L M	21 (0x0015)
M M L	22 (0x0016)
M M H	23 (0x0017)
M H M	24 (0x0018)
H M M	25 (0x0019)
M M M	26 (0x001A)

Page29: MISC: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[10:0]		
L	L	L	00000	RAMCFG TRD	H=High :Tied to 1.8V
L	H	L	00010	RAMCFG TRD	M=Middle:Tied to 0.9V
L	L	H	00011	RAMCFG TRD	L=Low :Tied to 0V
H	H	L	00110	RAMCFG TRD	DEFAULT
L	L	H	00001	RAMCFG MICRON	

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN(2:0)_FS_OVERT	1-ENABLE 0-DISABLE	
H	H	H	0111	FS_OVERT ENABLE	DEFAULT
H	H	M	0000	FS_OVERT DISABLE	

STRAPS	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	1:SMB_ALT_ADDR ENABLE
M	H	L	1	1	1	0	0:SMB_ALT_ADDR DISABLE
M	L	H	1	1	0	1	1:DEVID_SEL RESBOARD
M	L	L	1	1	0	0	0:DEVID_SEL ORIGINAL
L	H	L	1	1	0	0	1:PCIE_CFG LOW POWER
L	H	M	1	0	1	1	0:PCIE_CFG HIGH POWER
L	M	H	1	0	1	0	1:VGA_DEVICE ENABLE
L	M	L	1	0	0	1	0:VGA_DEVICE DISABLE
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	L	H	0	0	1	1	
L	L	M	0	0	1	0	
L	H	L	0	0	1	1	
L	H	M	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	

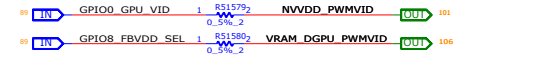
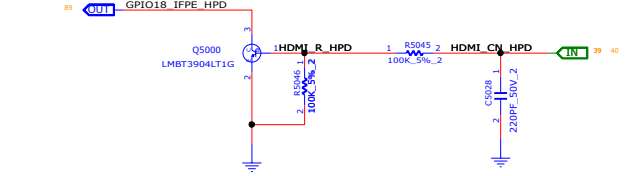
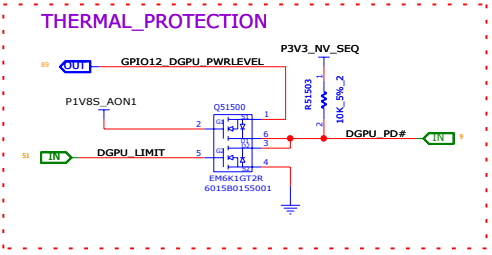
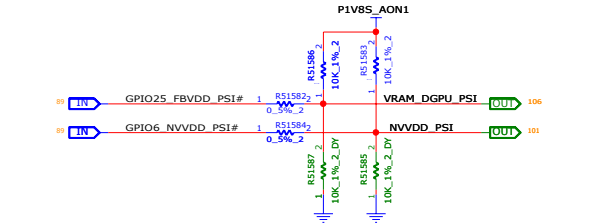
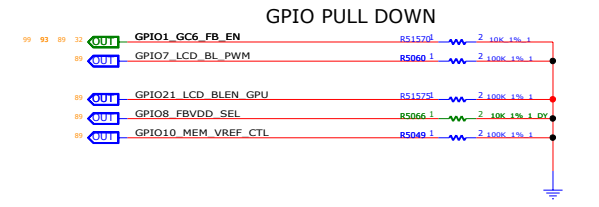
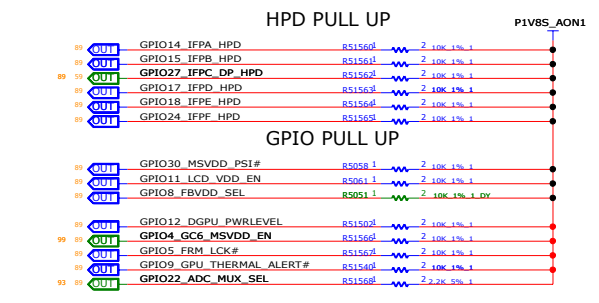
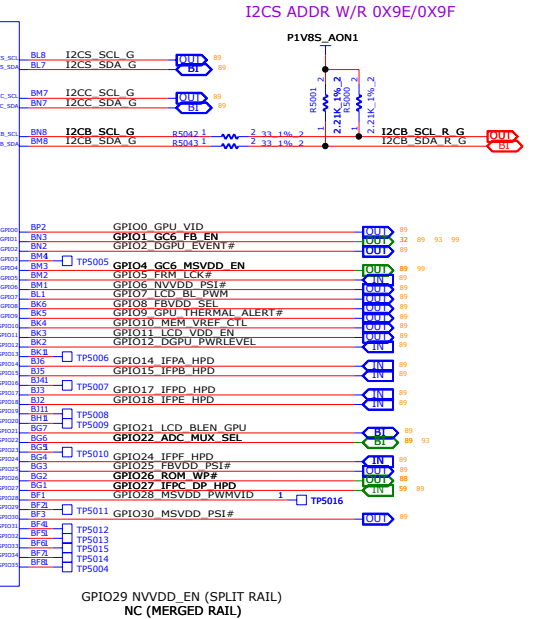
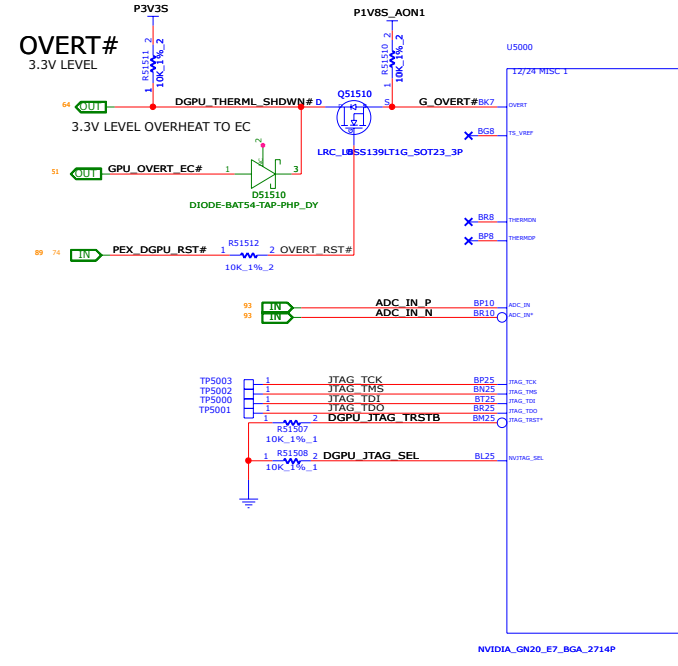
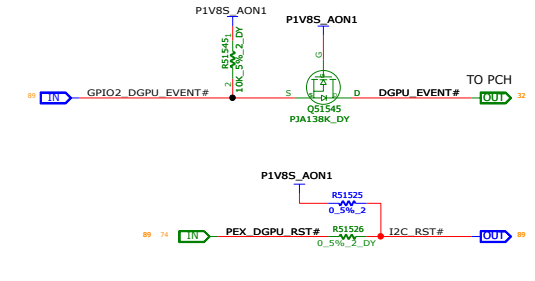
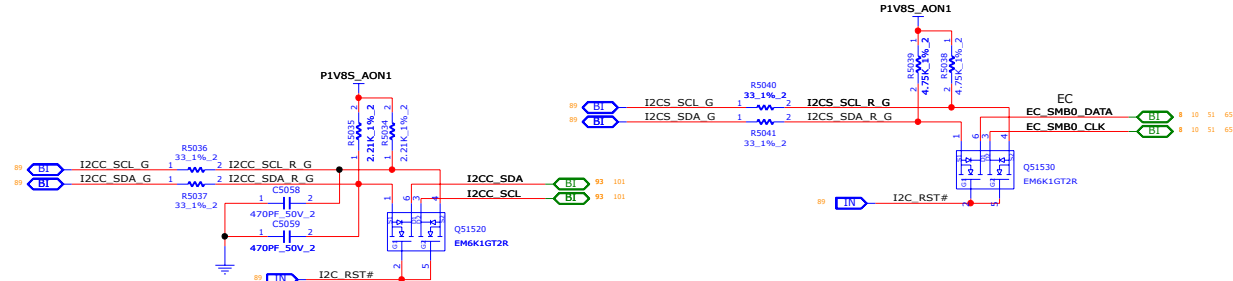
<https://realschematic.com>

INVENTEC

TITLE	MODEL_PROJECT,FUNCTION	SIZE	REV
Block	Diagram	A1	X01
CODE	1310xxxx-B-B	DATE	21-OCT-2002
CS		DATE	21-OCT-2002
CHG	XXX	DATE	21-OCT-2002
PCB P/N	6Pxxxxxxxxxx	PCB VER	XXX
SHEET	88	of	110

GPU GPIO

LOCATION NUMBER : 5000~5499, 51500~51599

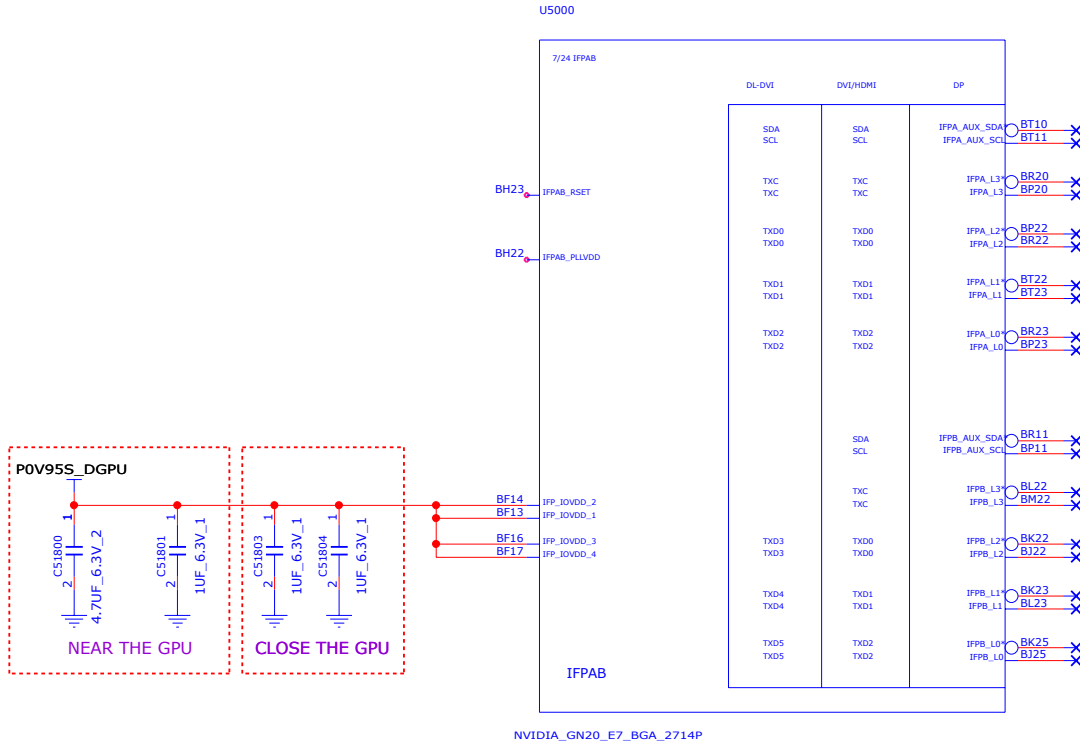


INVENTEC

CHANGE ID	XXX	DATE	21-OCT-2002	SIZE	CODE	DOC NUMBER	REV
P/CB P/N	6Pxxxxxxxxxxxx	P/CB VER	XXX	SHEET	81	116	X01

GPU IFP_AB

LOCATION NUMBER : 5000~5499, 51800~51899

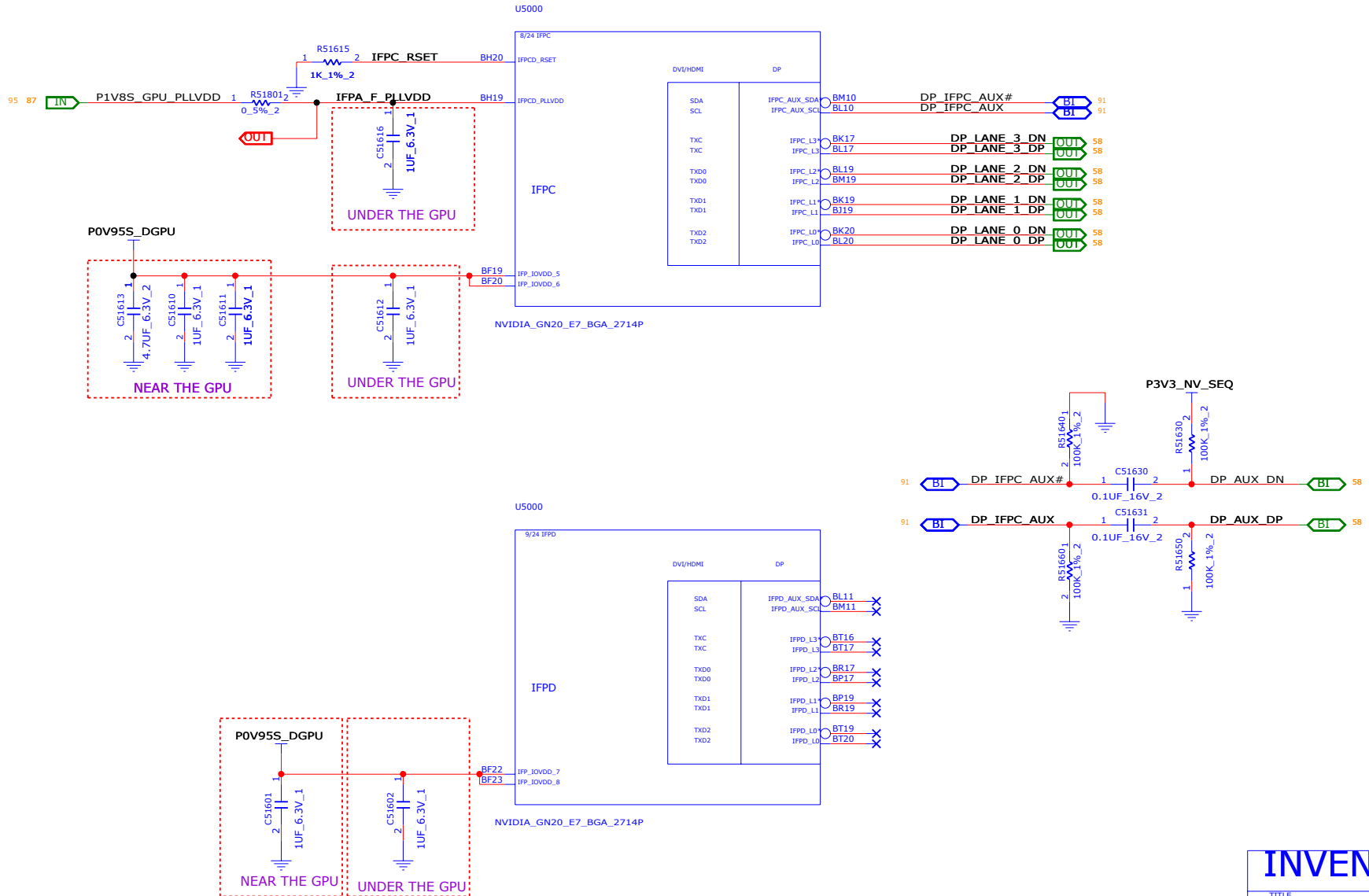


NVIDIA_GN20_E7_BGA_2714P

INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC. NUMBER 1310xxxx-0-0	REV X01
CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
SHEET		90 of 119	

GPU IFP_CD(DP)

LOCATION NUMBER : 5000~5499, 51600~51699



<https://realschematic.com>

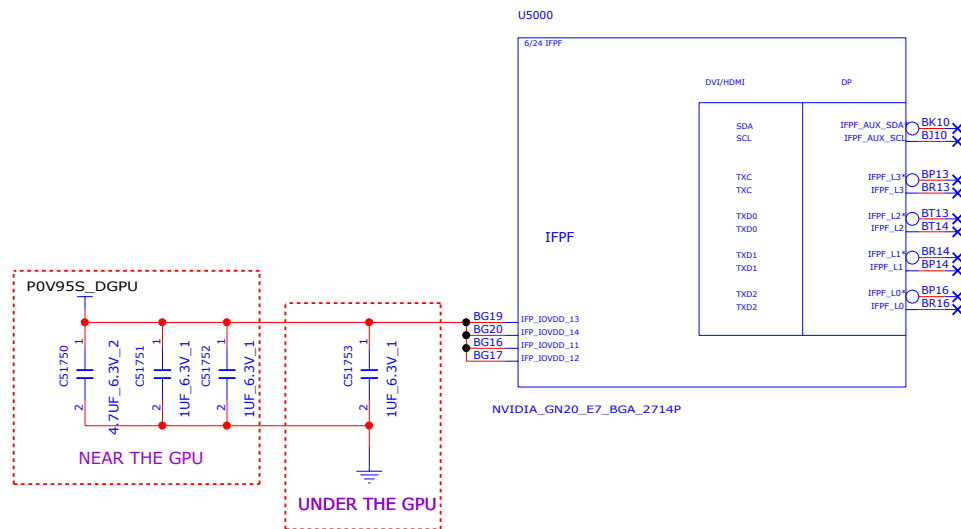
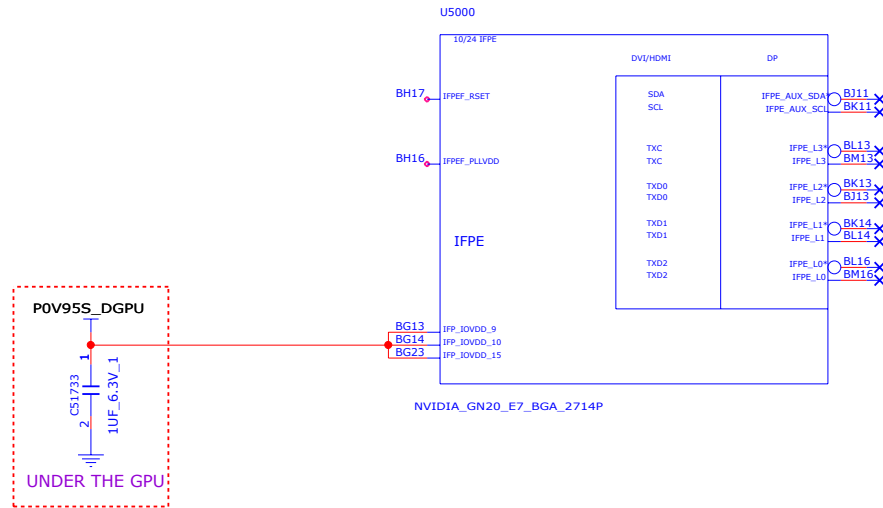
INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by		DATE	
PCB P/N		PCB VER	
XXX		21-OCT-2002	
60xxxxxxxxxxx		XXX	
SHEET	91 of 119		

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX
SHEET	91 of 119		

GPU IFP_EF

LOCATION NUMBER : 5000~5499, 51700~51799



<https://realschematic.com>

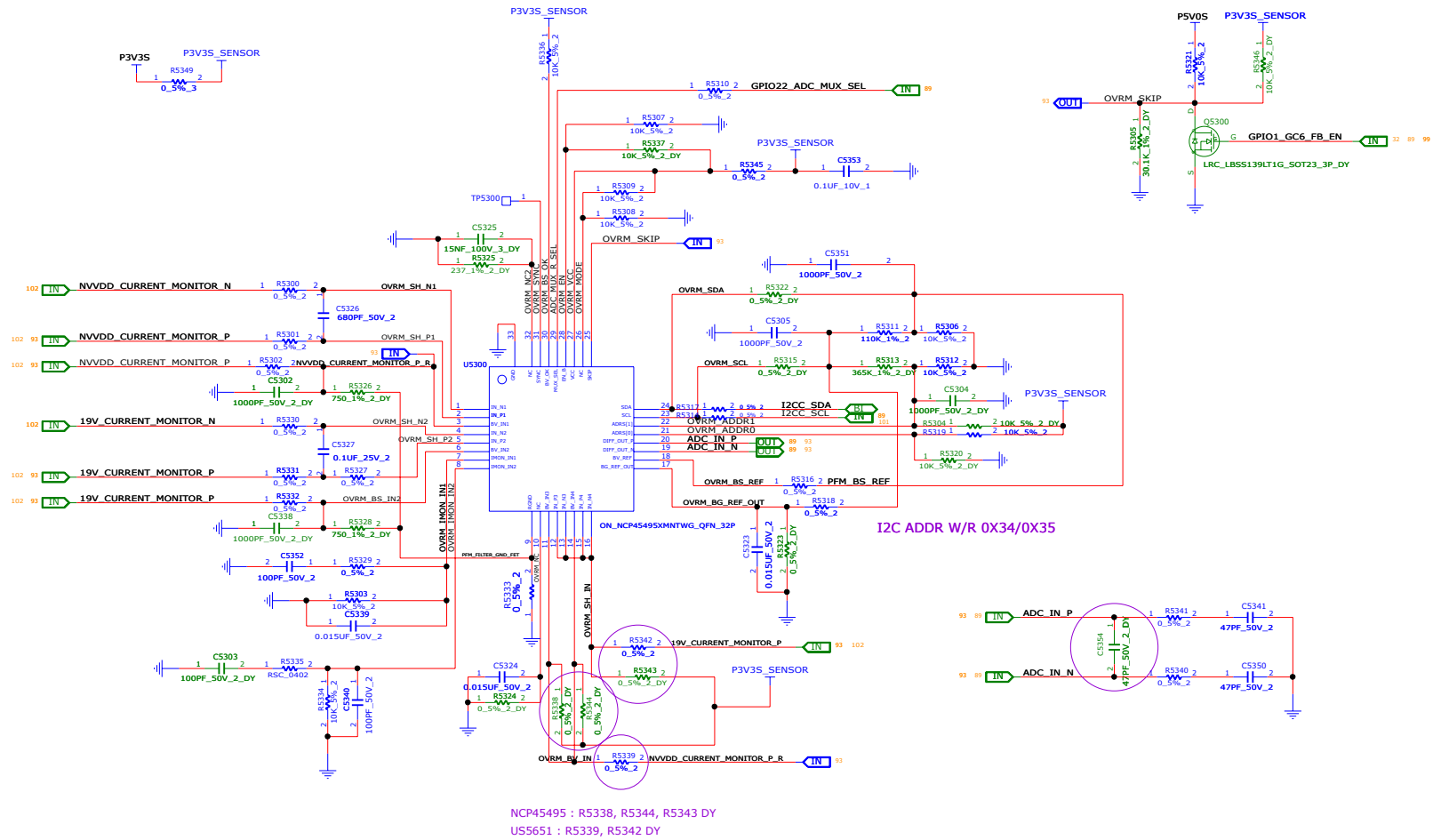
INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION		Block Diagram	
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET		92 of 119	

CHANGE BY	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER.	XXX

OVR-M NCP45495 & US5651(COALY)

LOCATION NUMBER : 5300~5399(NCP45495)

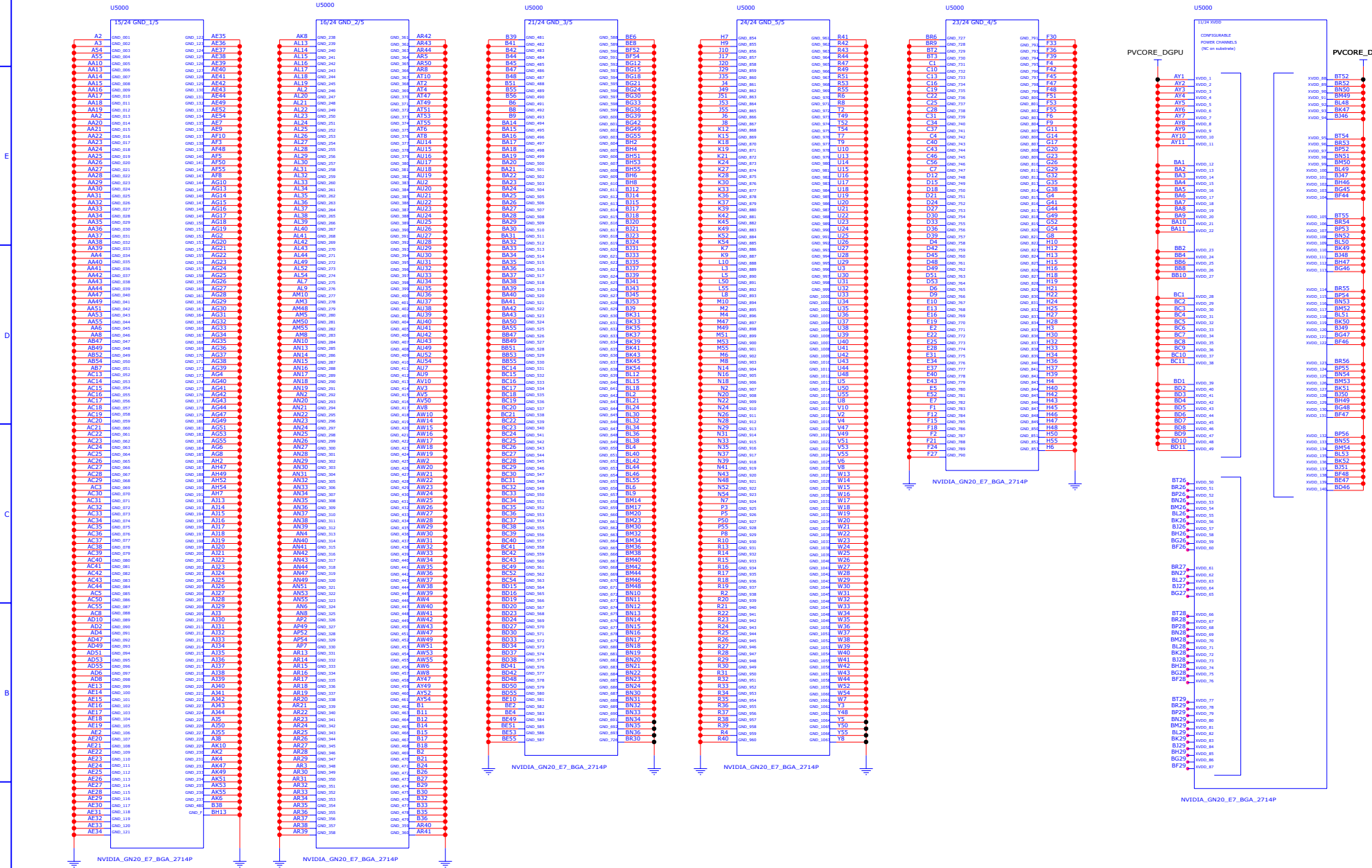


<https://realschematic.com>

INVENTEC	
TITLE	MODEL_PROJECT_FUNCTION
Block	Diagram
SIZE	DOC NUMBER
A1	13110xxxx-B-B
SHEET	REV
31	X01
CHANGE BY	DATE
PCB P/N	PBR VER
XXX	21-OCT-2002
6Pxxxxxxxxxxx	XXX

GPU GND

LOCATION NUMBER : 5000-5499



<https://realschematic.com>

INVENTEC

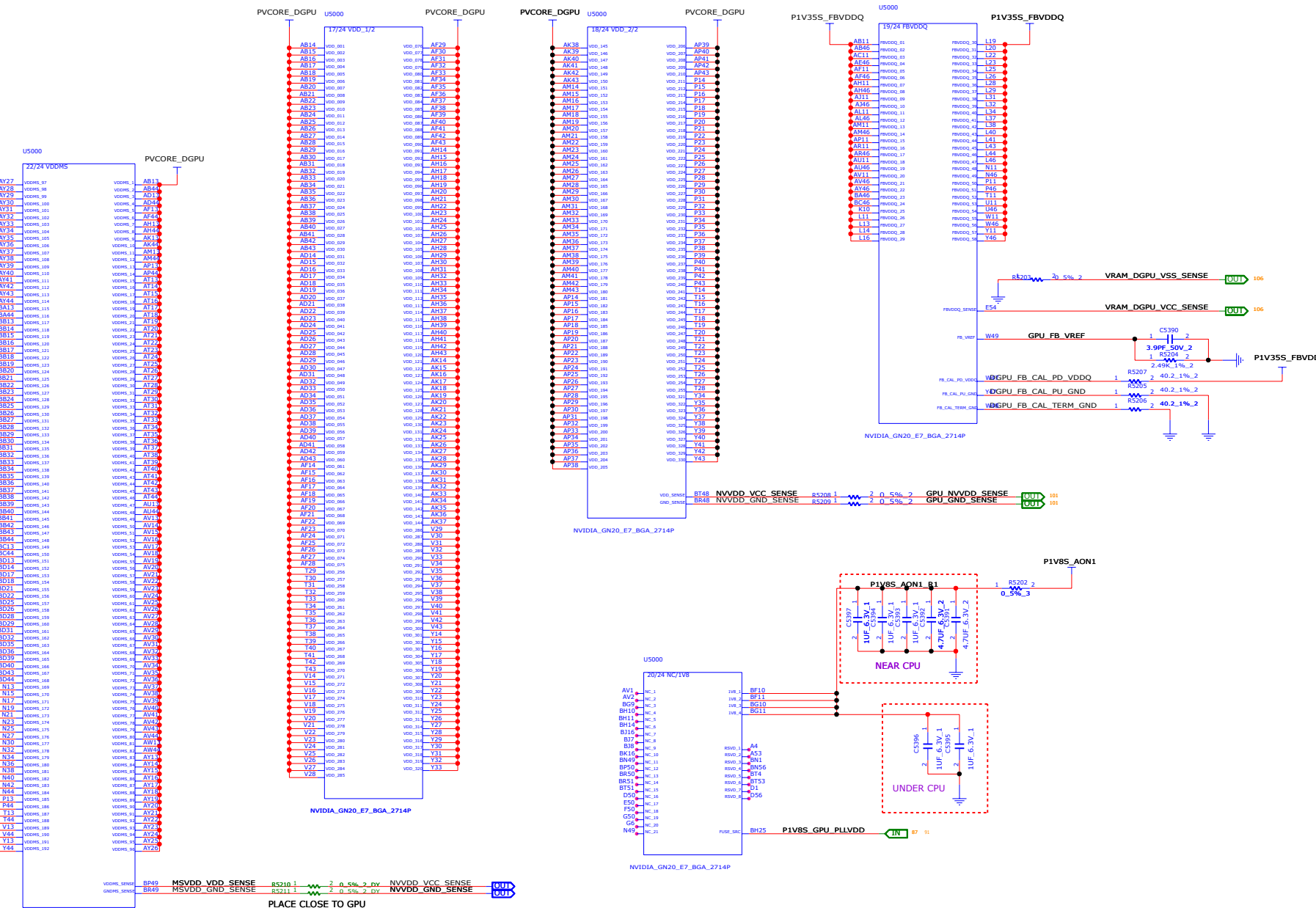
TITLE: MODEL_PROJECT_FUNCTION
Block Diagram

CHANGE IN	XXX	DATE	21-OCT-2002	SIZE	A1	CODE	CS	1310XXXXX-D-B	REV	X01
PCB P/N	6PXXXXXXXXXX	PCB VER	XXX	SHEET	34	OF	110			

GPU POWER

LOCATION NUMBER : 5000-5499

F
E
D
C
B
A



U5000_Sense01 BR49 MSVDD VDD SENSE R5210 1 2 0 50k 2 DV NVDD VCC SENSE (OUT) (OUT)
 U5000_Sense02 BR49 MSVDD GND SENSE R5211 1 2 0 50k 2 DV NVDD GND SENSE (OUT) (OUT)

PLACE CLOSE TO GPU

NVidia_GN20_E7_BGA_2714P

<https://realschematic.com>

INVENTEC

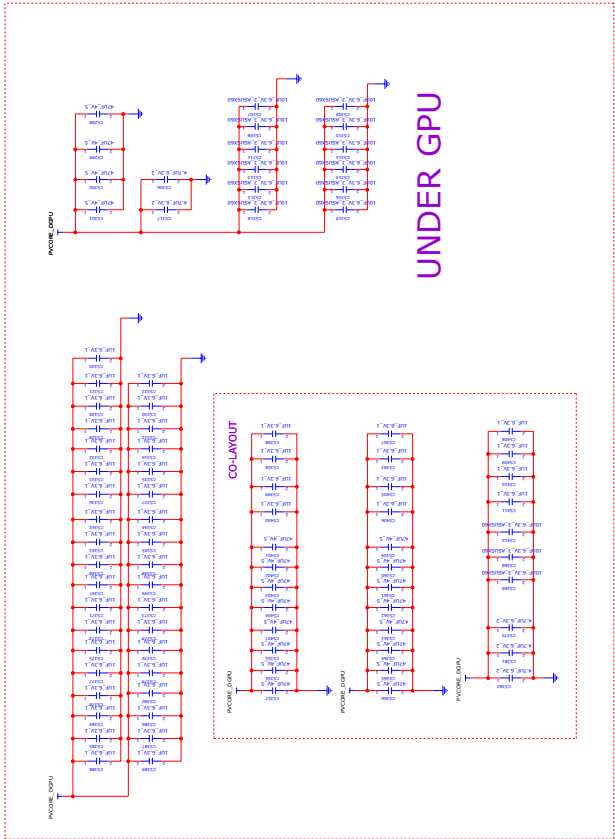
TITLE MODEL_PROJECT,FUNCTION
Block Diagram

SIZE 61 CODE CS 13104xxxx-B-0
REV X01

CHANGE IN XXX	DATE 21-OCT-2002
PCB P/N 6P0xxxxxxx	PCB VER XXX
SHEET 35	TOTAL 110

GPU NVVDD DECOUPLING

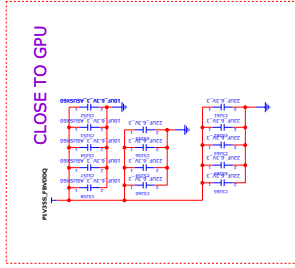
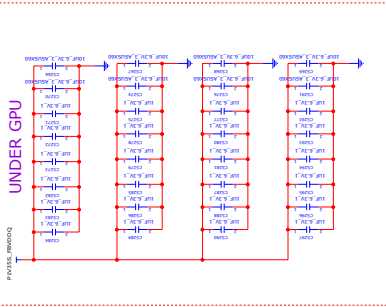
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GPU FBVDDQ DECOUPLING

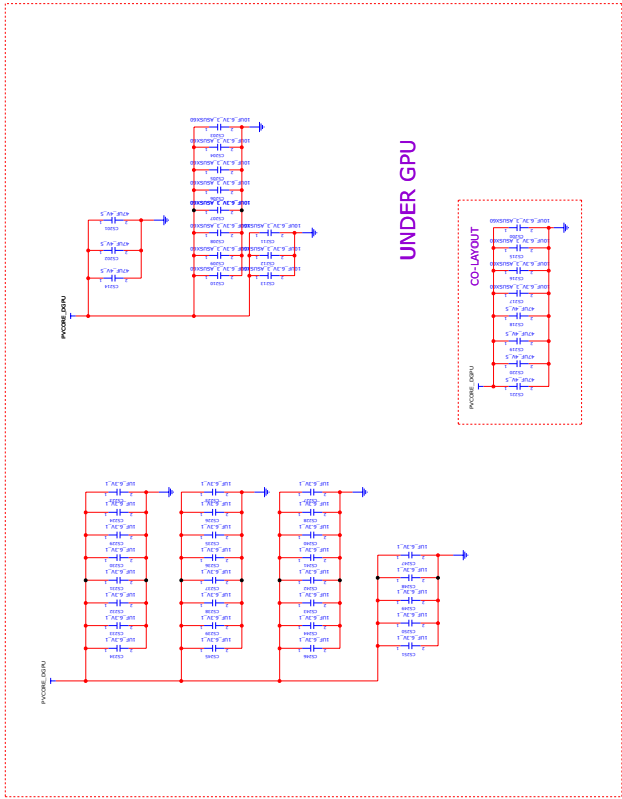
LOCATION NUMBER: 1000-5699

<https://realschematic.com>



GPU MSVDD DECOUPLING

LOCATION NUMBER: 1.000-5491

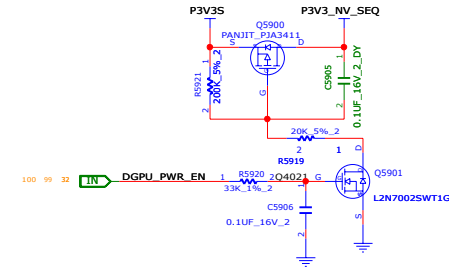


<https://realschematic.com>

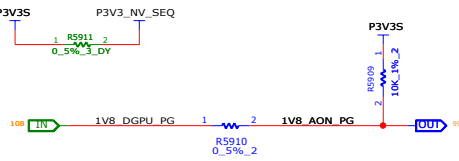
GPU POWER SEQUENCE

LOCATION NUMBER : 5900~5999

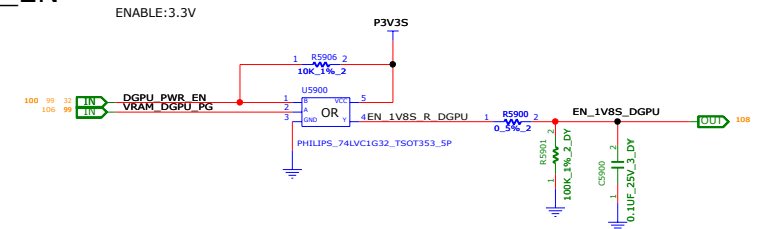
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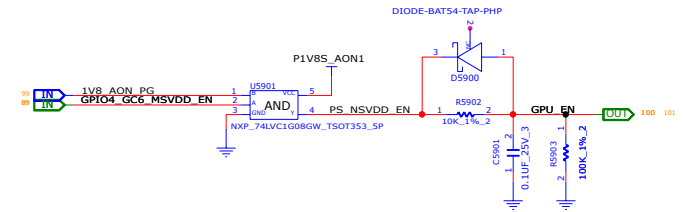
DGPU_1V8_PG



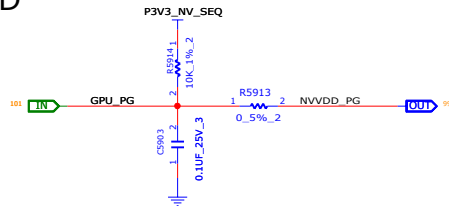
1V8_AON_EN



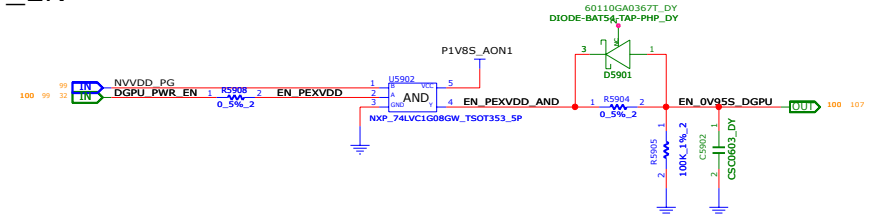
NVDD_EN



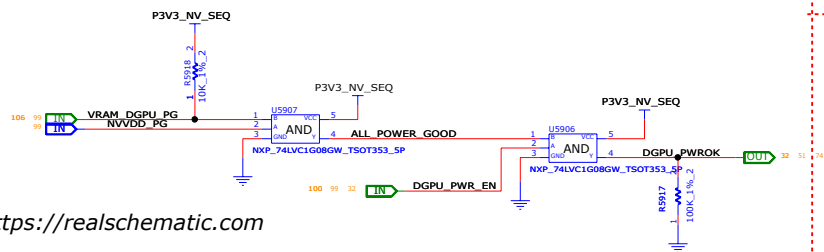
NVDD_PGOOD



PEX_VDD_EN

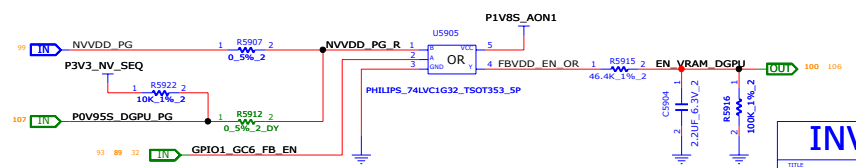


ALL POWER GOOD



FBVDD_EN

FOR GC6 3.0



<https://realschematic.com>

INVENTEC

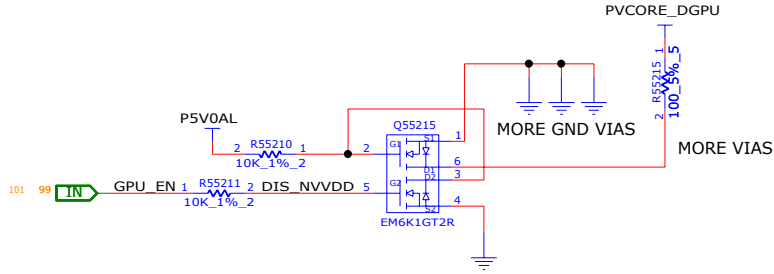
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE ID	XXX	DATE	21-OCT-2002	SIZE	CODE	DOC NUMBER	REV
PCB P/N	6Pxxxxxxxxxxxx	PCB VER	XXX	SHEET	35	of 116	1

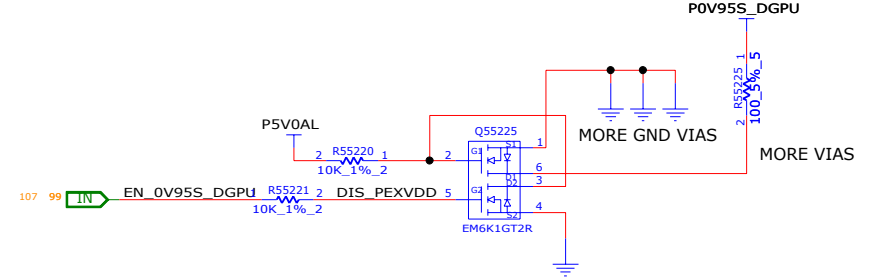
GPU POWER DISCHARGE

LOCATION NUMBER : 55200~55299

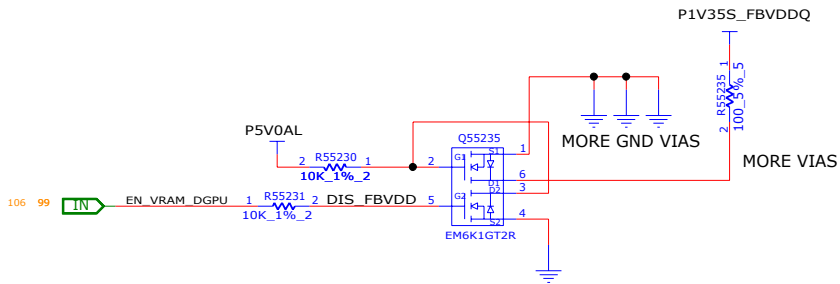
NVVD DISCHARGE



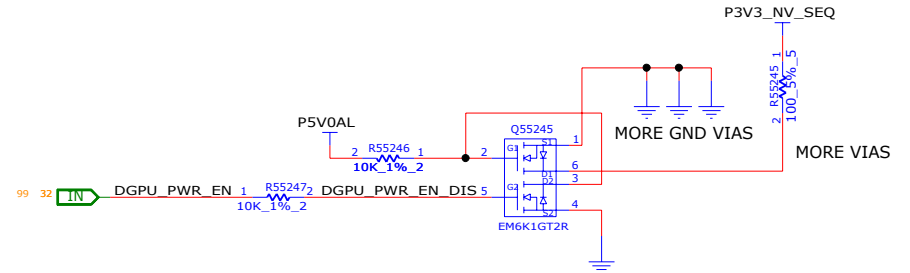
PEXVDD DISCHARGE



FBVDD DISCHARGE



P3V3_NV_SEQ DISCHARGE



<https://realschematic.com>

INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

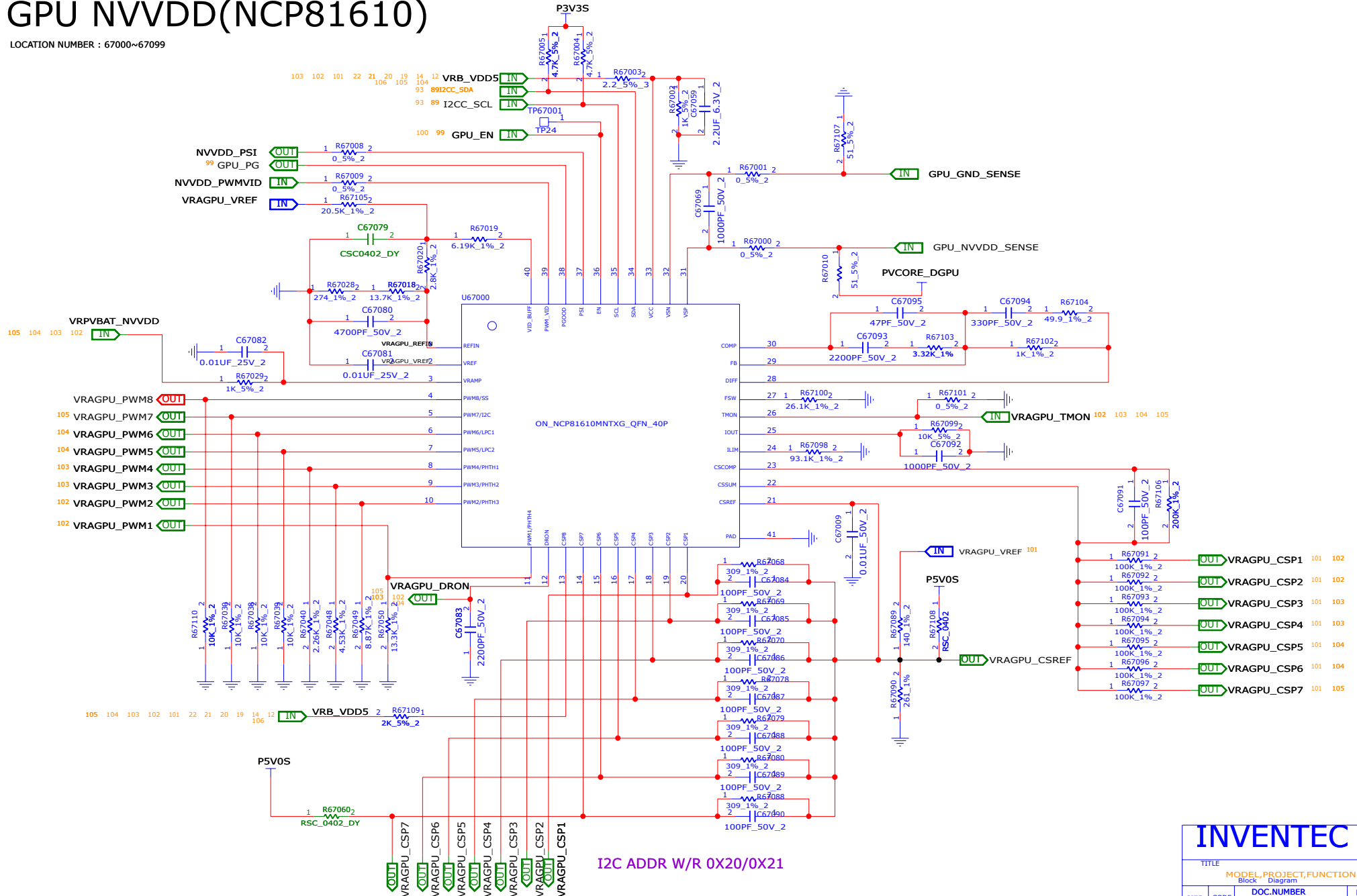
SIZE A3 CODE CS 1310xxxxx-0-0 REV X01

SHEET 100 of 119

CHANGE by: XXX DATE: 21-OCT-2002
PCB P/N: 60xxxxxxxxxxx PCB VER: XXXX

GPU NVVDD(NCP81610)

LOCATION NUMBER : 67000~67099



I2C ADDR W/R 0X20/0X21

<https://realschematic.com>

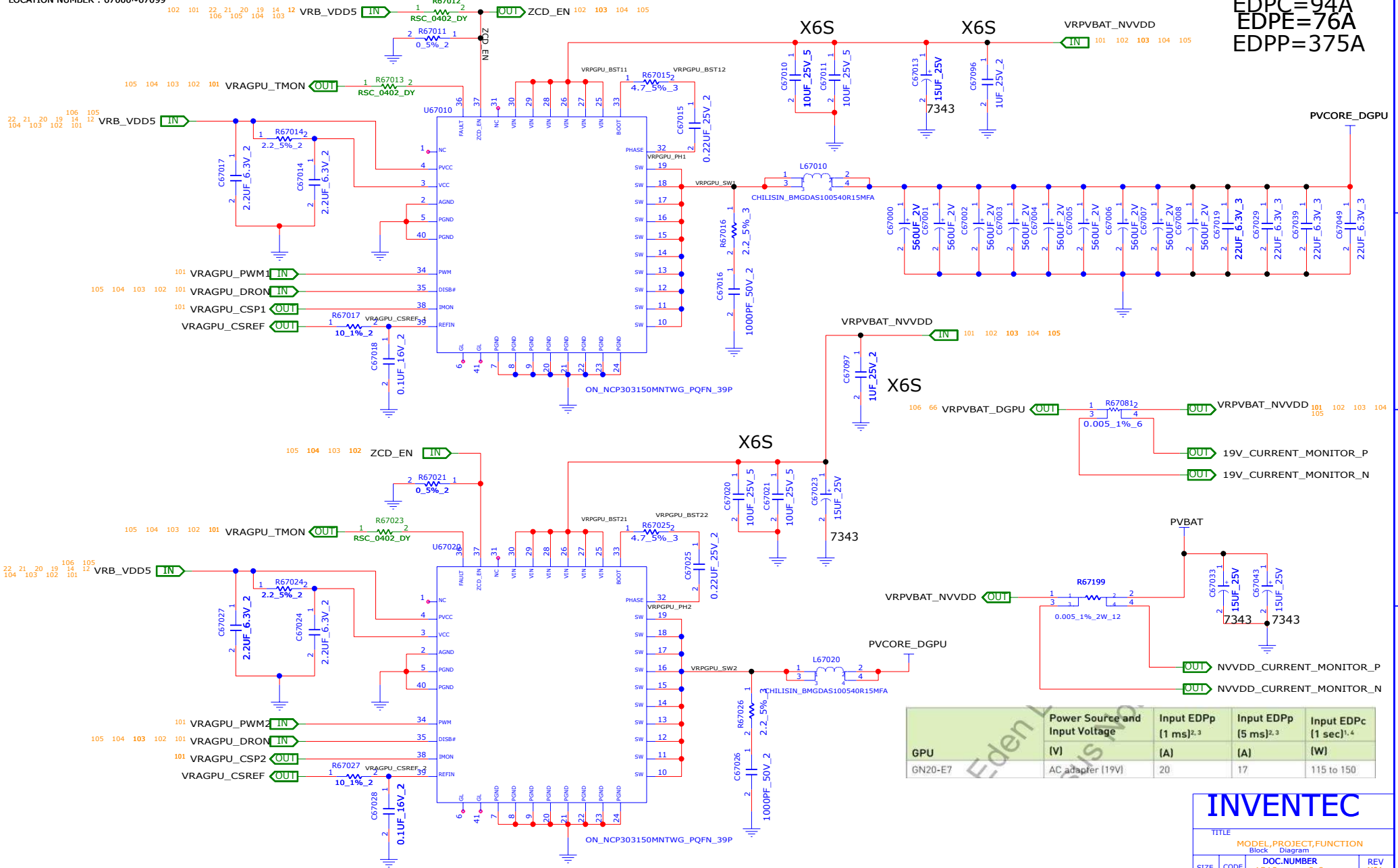
INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	
PCB P/N 60xxxxxxxxxx		PCB VER XXX	
SHEET 101 of 119			

PVCORE_DGPU (NCP303150_1-2P)

LOCATION NUMBER : 67000~67099

GN20-E7 115W
EDPC=94A
EDPE=76A
EDPP=375A



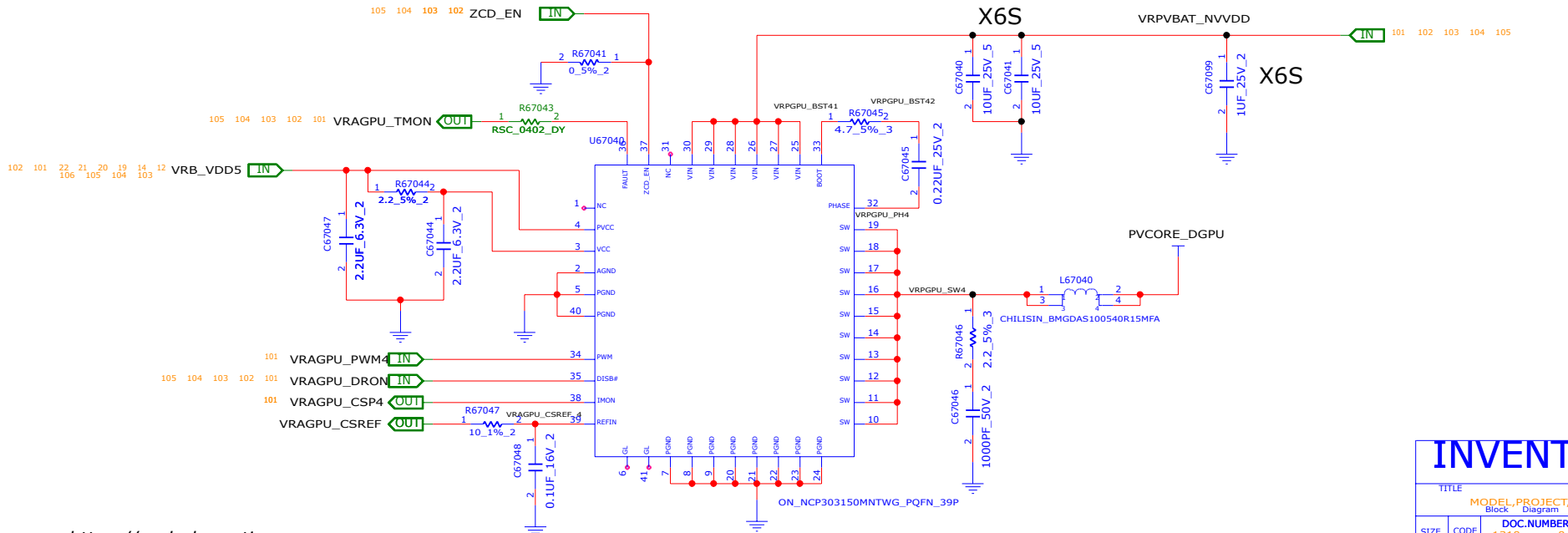
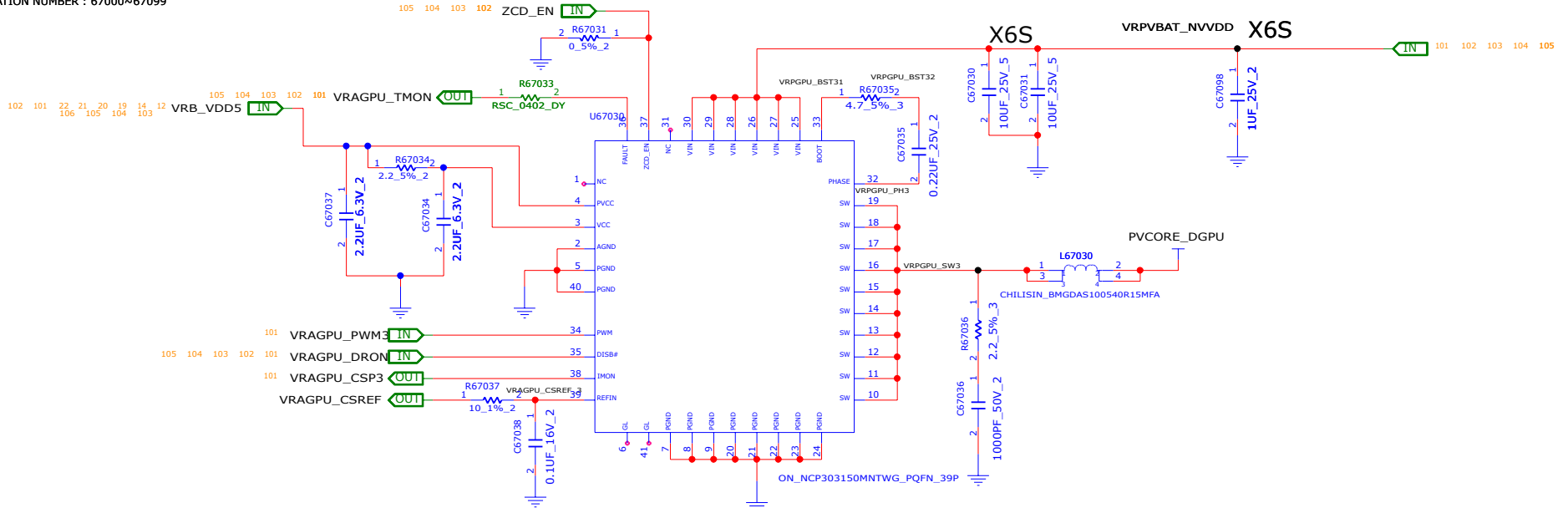
GPU	Power Source and Input Voltage		Input EDPP (1 ms) ^{2,3}	Input EDPP (5 ms) ^{2,3}	Input EDPP (1 sec) ^{1,4}
	(V)	(A)	(A)	(A)	(W)
GN20-E7	AC adapter (19V)	20	17	115 to 150	

INVENTEC			
TITLE MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
CHANGE PCB P/N	DATE PCB VER	DATE 21-OCT-2002	SHEET 102 of 119

<https://realschematic.com>

PVCORE_DGPU (NCP303150_3-4P)

LOCATION NUMBER : 67000~67099

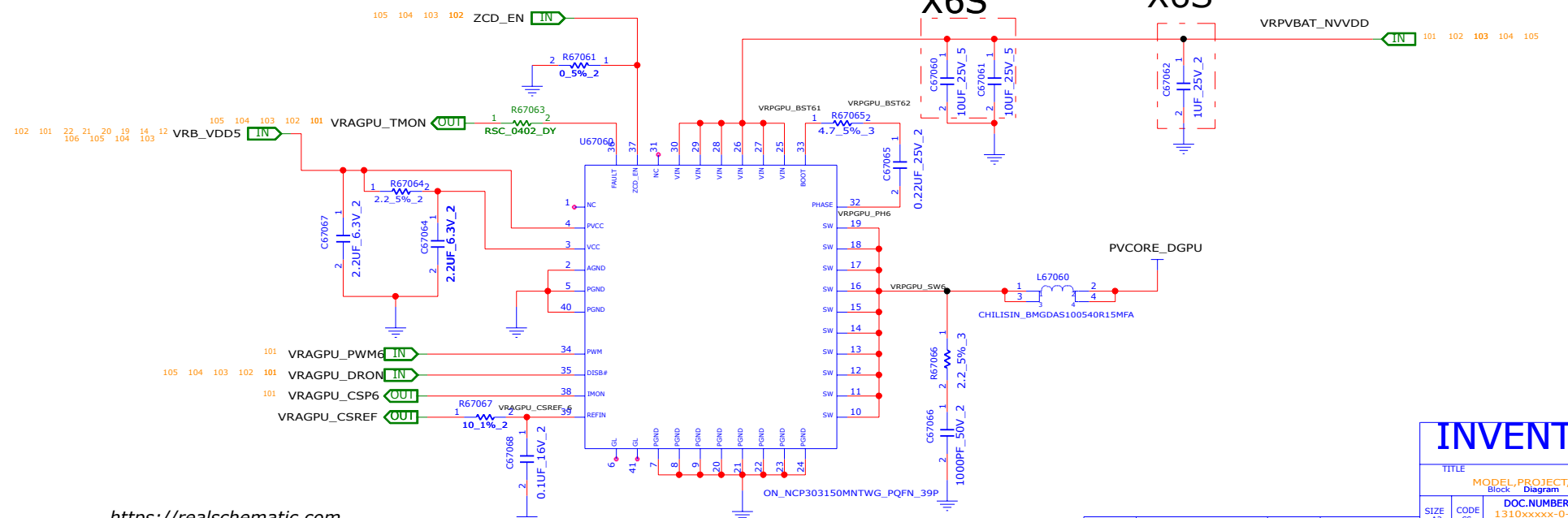
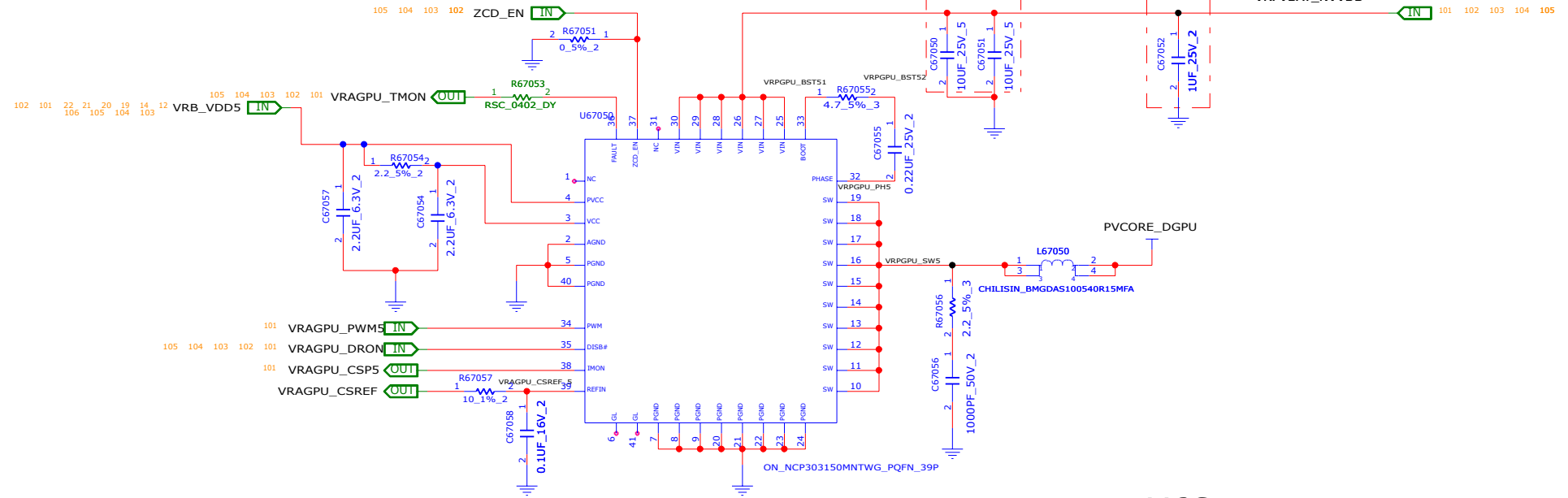


<https://realschematic.com>

INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by		DATE	
PCB P/N		PCB VER	
XXX		21-OCT-2002	XXX
SHEET		103 of 119	

PVCORE_DGPU (NCP303150_5-6P)

LOCATION NUMBER : 67000~67099

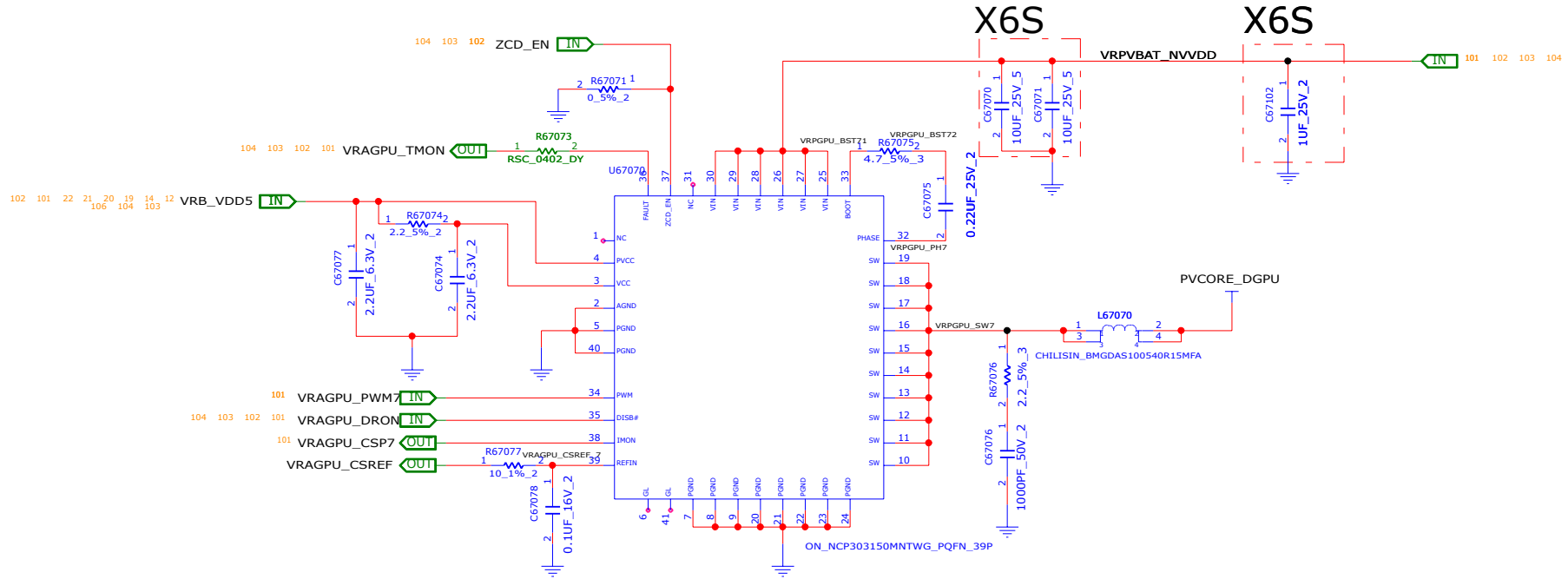


<https://realschematic.com>

INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by		DATE	
PCB P/N		PCB VER	
XXX		21-OCT-2002	XXX
SHEET		104 of 119	

PVCORE_DGPU (NCP303150_7P)

LOCATION NUMBER : 67000~67099



INVENTEC

TITLE
MODEL, PROJECT, FUNCTION
Block Diagram

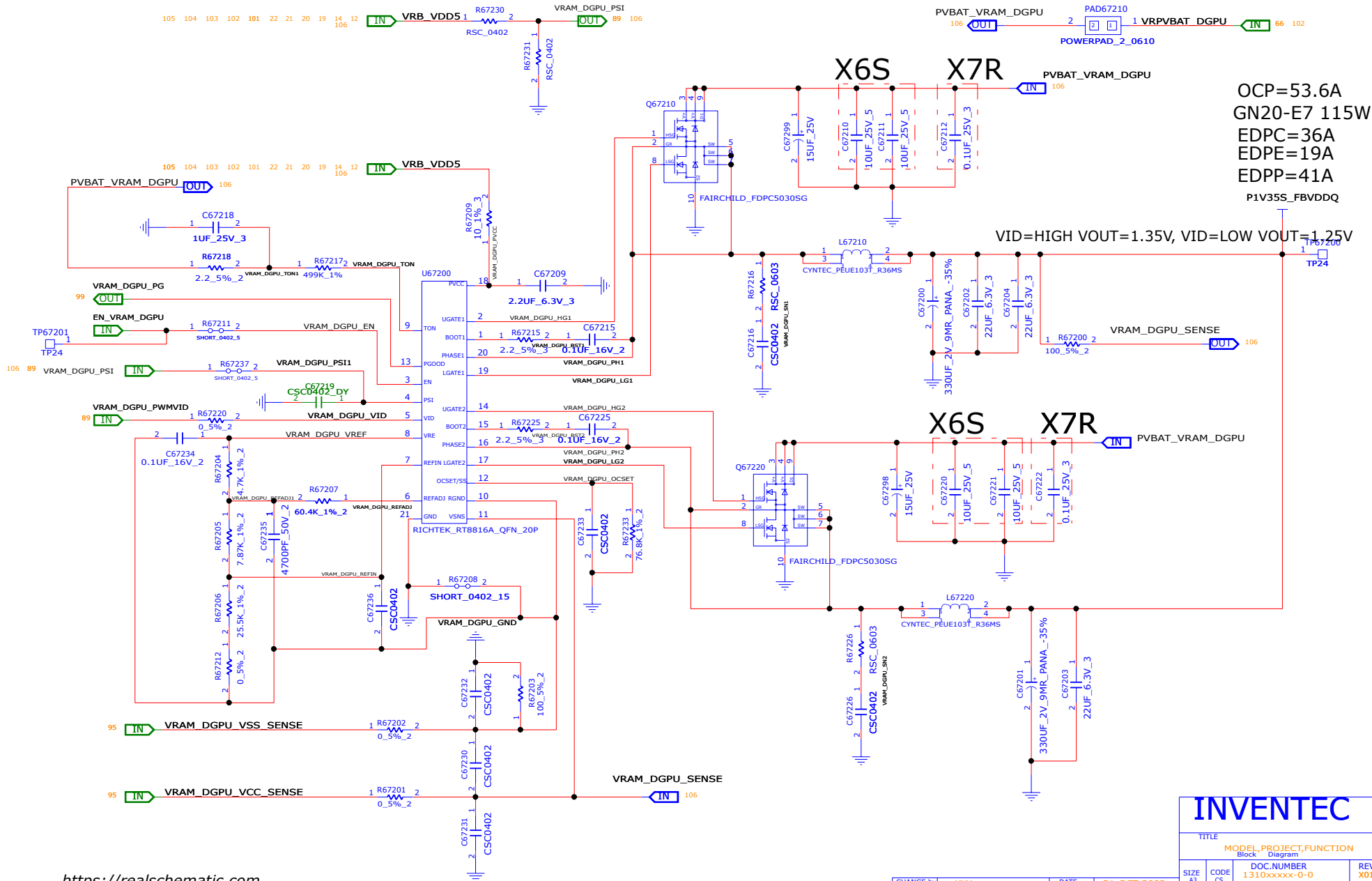
SIZE A3 CODE CS 1310xxxx-0-0 REV X01

DOC. NUMBER 105 of 119

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

P1V35S_DGPU (RT8816A_2P)

LOCATION NUMBER : 67200~67299



OCP=53.6A
 GN20-E7 115W
 EDPC=36A
 EDPE=19A
 EDPP=41A
 P1V35S_FBVDQ

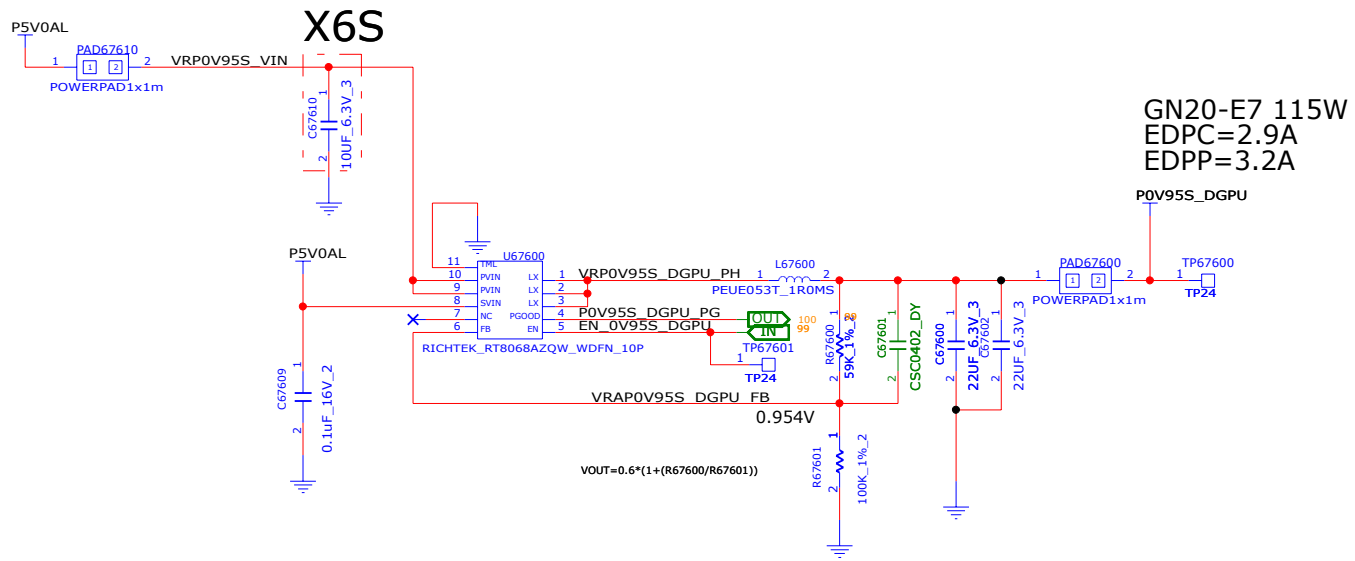
VID=HIGH VOUT=1.35V, VID=LOW VOUT=1.25V

INVENTEC				
TITLE	MODEL, PROJECT, FUNCTION			
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxxx-0-0	REV X01	
SHEET 106				of 119

CHANGE BY	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

P0V95S_DGPU (RT8068A)

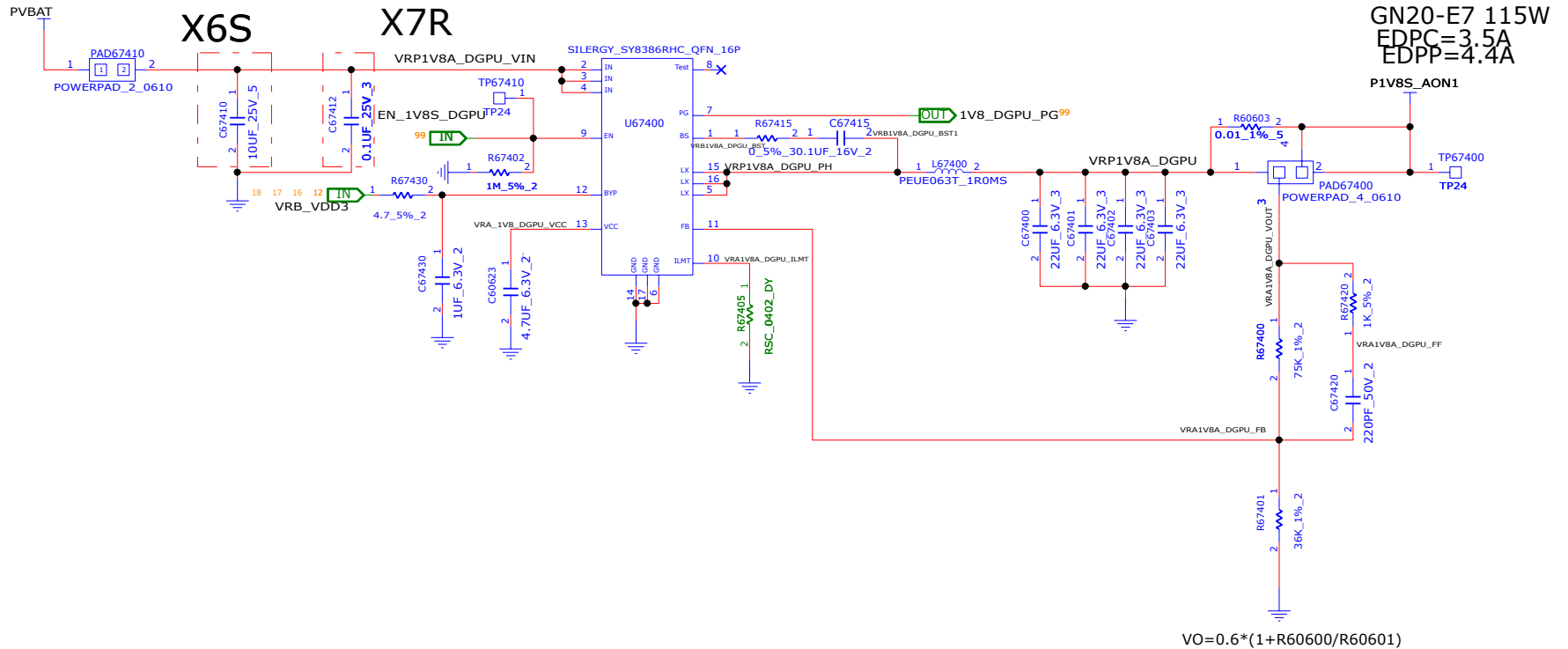
LOCATION NUMBER : 67600~67699



INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by	DATE	DATE	DATE
PCB P/N	60xxxxxxxxxx	21-OCT-2002	XXX
		PCB VER.	
		XXX	
SHEET	107 of 119		

P1V8S_AON1 (SY8386)

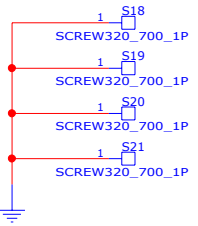
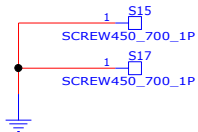
LOCATION NUMBER : 67400~67499



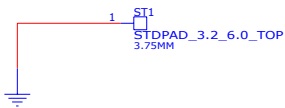
INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE BY	DATE	PCB VER	SHEET
XXX	21-OCT-2002	XXX	108 of 119
PCB P/N			

PCB SCREW / MASK / STANDOFF

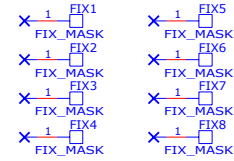
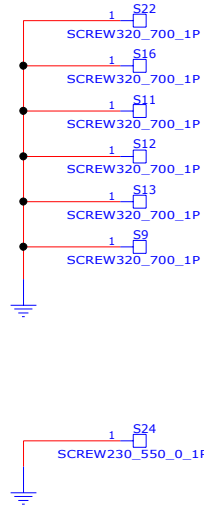
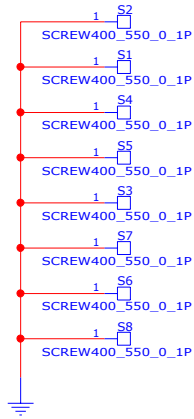
LOCATION NUMBER : 0~49



FOR PCIE



GPU CPU



INVENTEC			
TITLE			
MODEL		PROJECT/FUNCTION	
XDP & RE		CONN.	
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE BY	DATE	PCB VER.	SHEET
XXX	21-OCT-2002	XXX	109 of 119
PCB P/N	60xxxxxxxxxx		

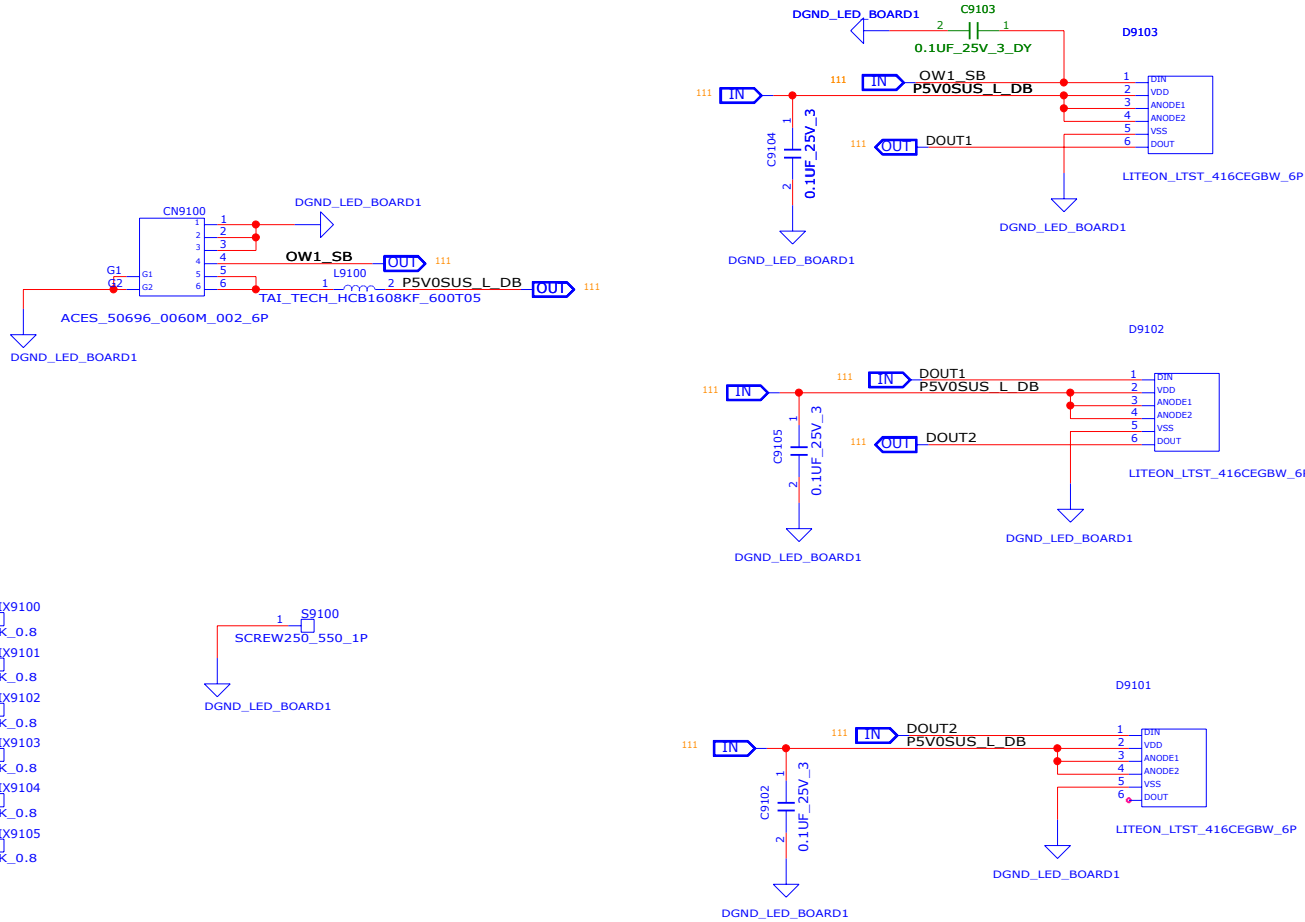
DB BOARD

PAGE110-118

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	SHEET
XXX 60xxxxxxxxxxx		21-OCT-2002 XXX	110 of 119

L-U-BAR BOARD

LOCATION NUMBER : 9100~9124



<https://realschematic.com>

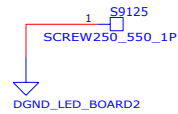
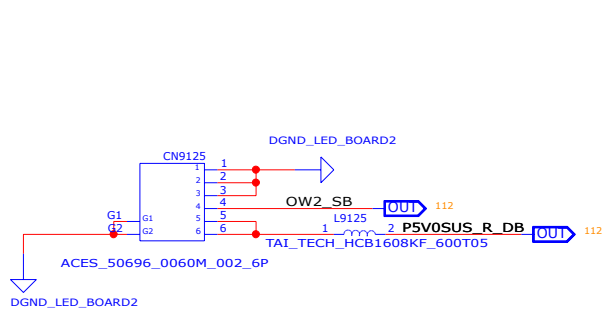
INVENTEC

TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET		111 of 119	

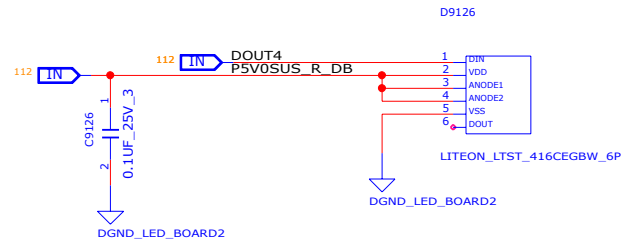
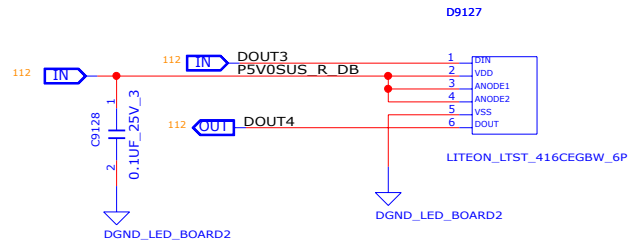
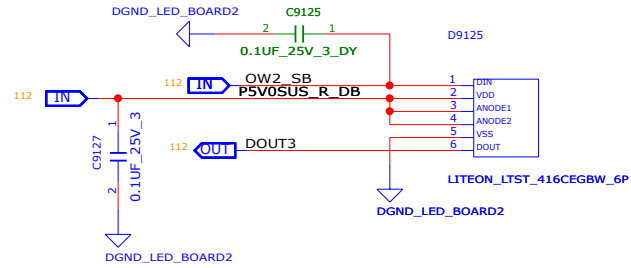
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

R-U-BAR BOARD

LOCATION NUMBER : 9125~9149



- 1 FIX9126
FIX_MASK_0.8
- 1 FIX9128
FIX_MASK_0.8
- 1 FIX9127
FIX_MASK_0.8
- 1 FIX9129
FIX_MASK_0.8
- 1 FIX9130
FIX_MASK_0.8
- 1 FIX9125
FIX_MASK_0.8



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INVENTEC

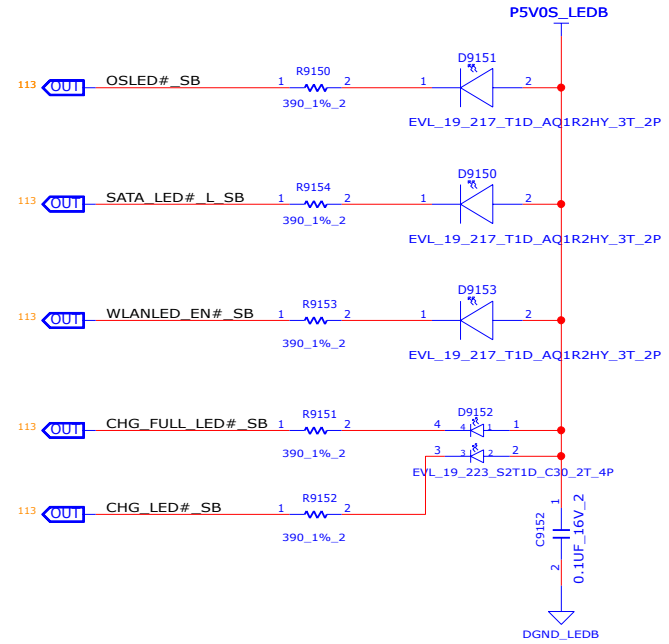
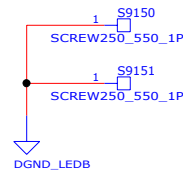
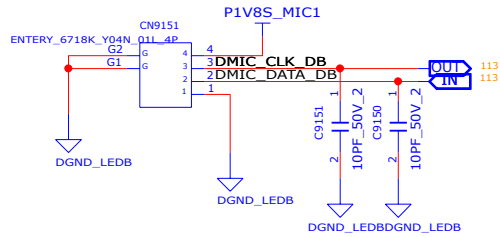
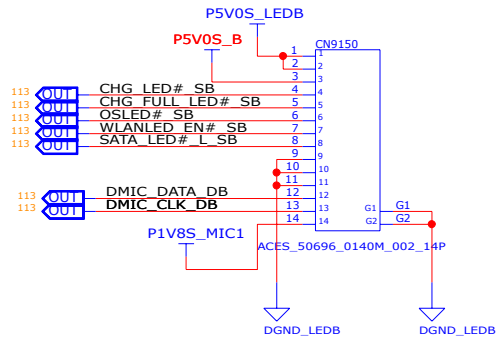
TITLE			
MODEL, PROJECT, FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
CHANGE by PCB P/N		DATE PCB VER	REV SHEET

CHANGE by: XXX
PCB P/N: 60xxxxxxxxxx
DATE: 21-OCT-2002
PCB VER: XXX

112 of 119

INDICATOR BOARD

LOCATION NUMBER : 9150~9199



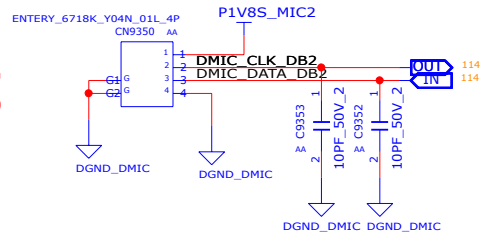
- X 1 FIX9152
FIX_MASK_0.8
- X 1 FIX9151
FIX_MASK_0.8
- X 1 FIX9153
FIX_MASK_0.8
- X 1 FIX9154
FIX_MASK_0.8
- X 1 FIX9150
FIX_MASK_0.8
- X 1 FIX9155
FIX_MASK_0.8

INVENTEC			
TITLE Block Diagram			
MODEL,PROJECT,FUNCTION		DOC.NUMBER	
1310xxxxx-0-0		REV X01	
CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
SIZE A3	CODE CS	SHEET 113 of 119	

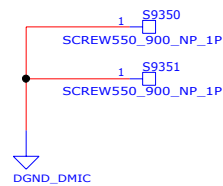
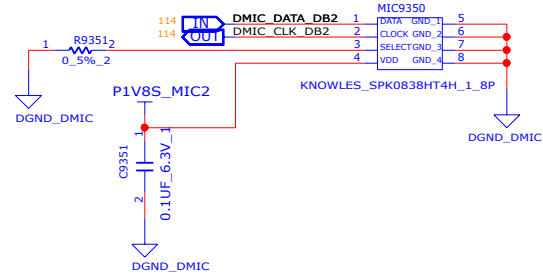
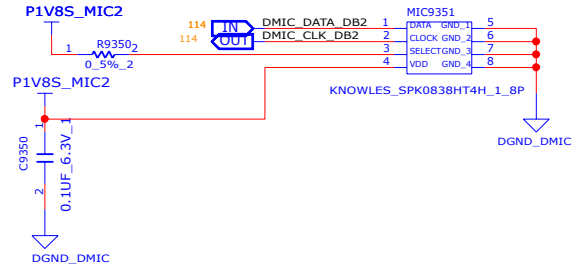
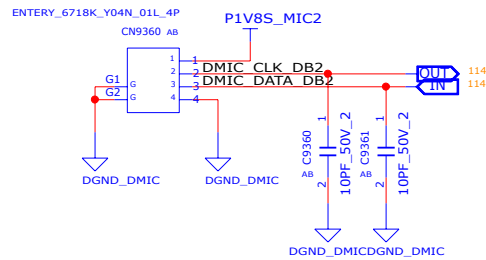
DMIC BOARD

LOCATION NUMBER : 9350~9399

G5



G7



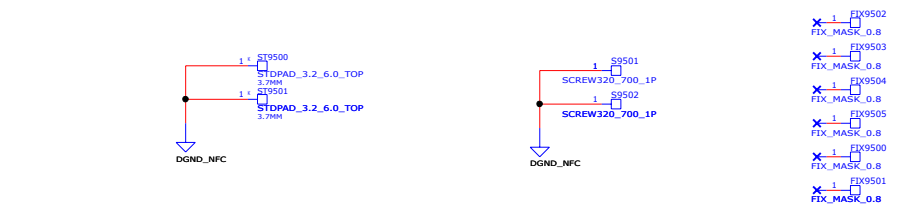
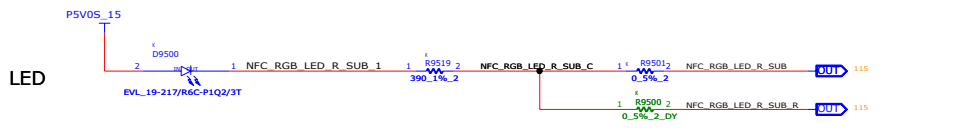
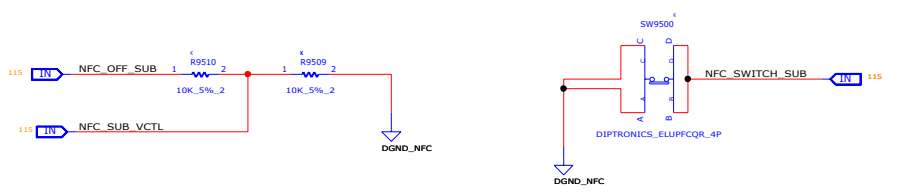
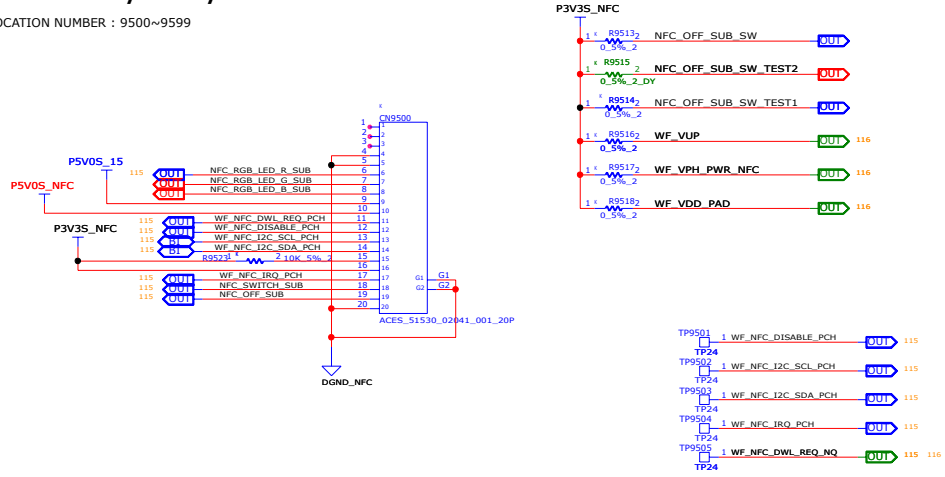
- X 1 FIX9355
- FIX_MASK_0.8
- X 1 FIX9350
- FIX_MASK_0.8
- X 1 FIX9351
- FIX_MASK_0.8
- X 1 FIX9352
- FIX_MASK_0.8
- X 1 FIX9353
- FIX_MASK_0.8
- X 1 FIX9354
- FIX_MASK_0.8

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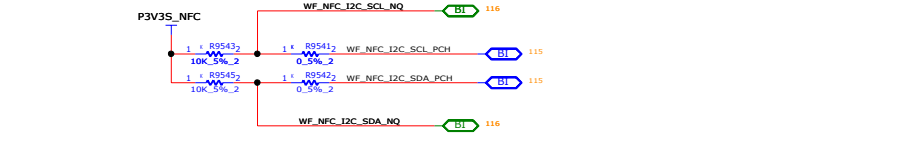
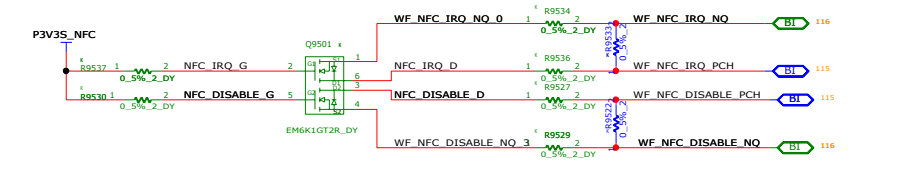
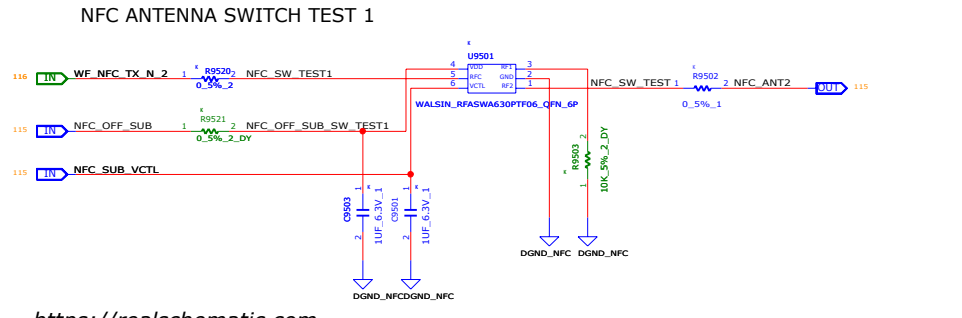
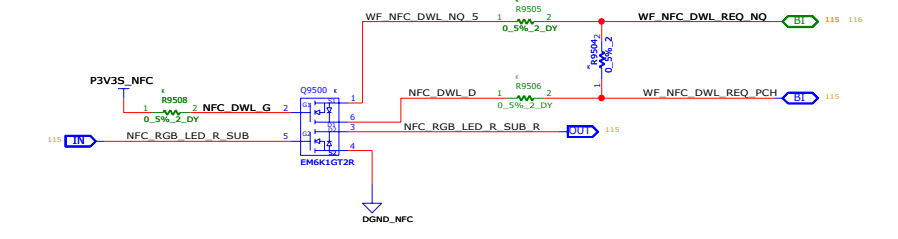
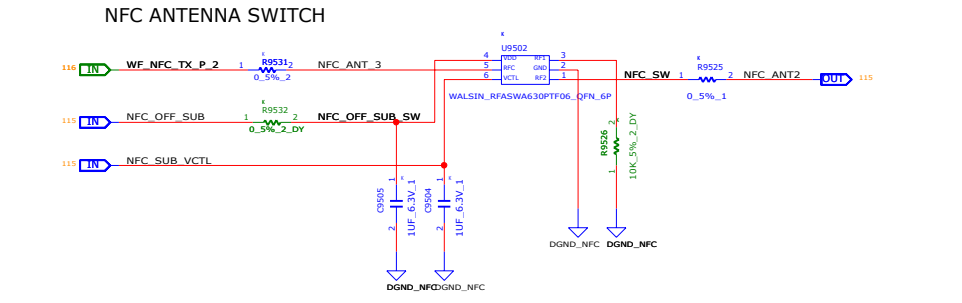
INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by	DATE	PCB VER.	SHEET
XXX	21-OCT-2002	XXX	114 of 119
PCB P/N	60xxxxxxxxxxx		

NFC CN/SW/LED

LOCATION NUMBER : 9500~9599



- FIX9502
- FIX_MASK_0.8
- FIX9503
- FIX_MASK_0.8
- FIX9504
- FIX_MASK_0.8
- FIX9505
- FIX_MASK_0.8
- FIX9500
- FIX_MASK_0.8
- FIX9501
- FIX_MASK_0.8



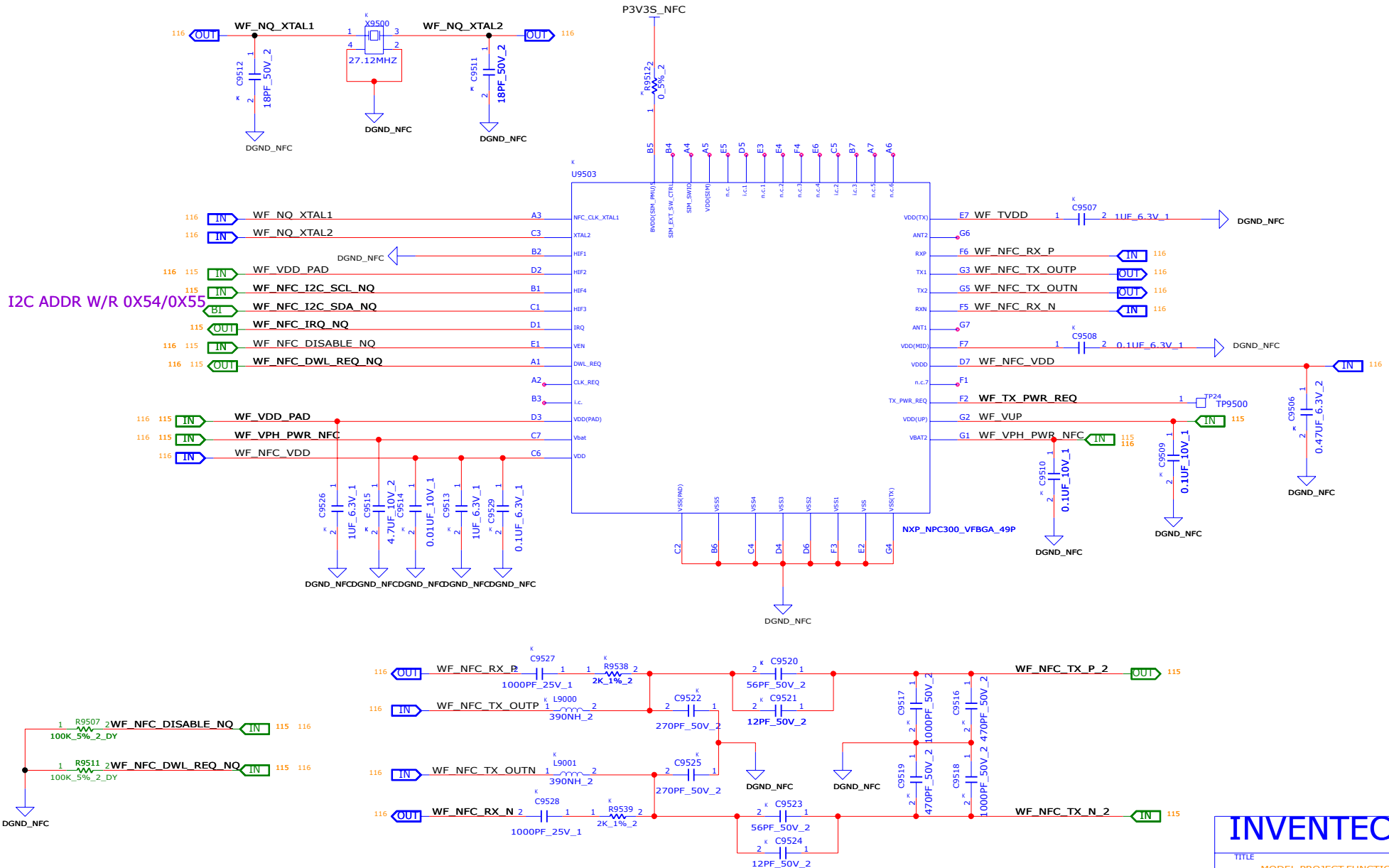
<https://realschematic.com>

INVENTEC

TITLE	MODEL_PROJECT,FUNCTION	SIZE	REV
RING_LED	1310xxxx-B-B	A1	X01
CHG	DATE	DATE	DATE
1	21-OCT-2002	1	1
PCB P/N	PCB VER	SHEET	115 of 115
6Pxxxxxxxxxx	xxxx	115	115

NFC IC

LOCATION NUMBER : 9500~9599

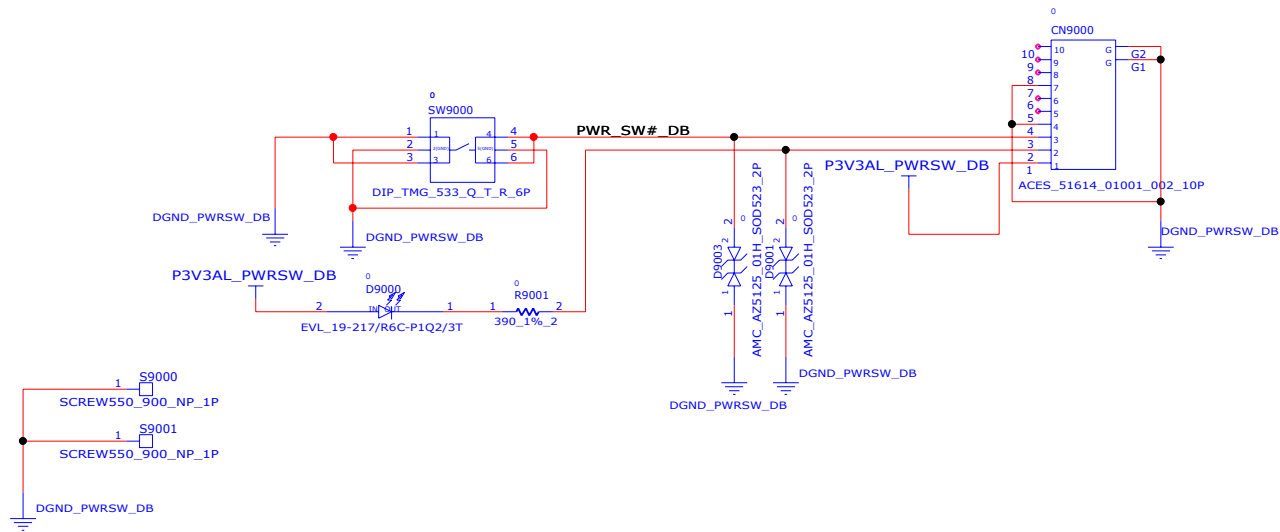


INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	
PCB P/N 60xxxxxxxxxxx		PCB VER XXX	
SHEET 116 of 119			

POWER KEY

LOCATION NUMBER : 9000~9050



- X 1 FIX9001
FIX_MASK_0.8
- X 1 FIX9002
FIX_MASK_0.8
- X 1 FIX9003
FIX_MASK_0.8
- X 1 FIX9004
FIX_MASK_0.8
- X 1 FIX9005
FIX_MASK_0.8
- X 1 FIX9000
FIX_MASK_0.8

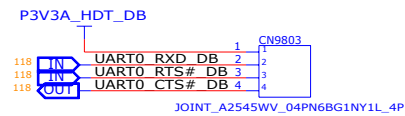
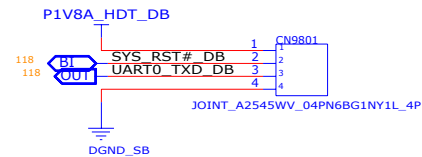
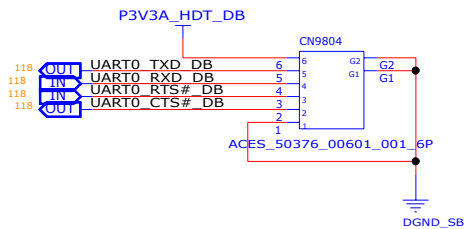
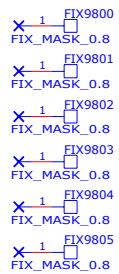
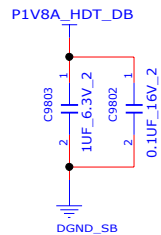
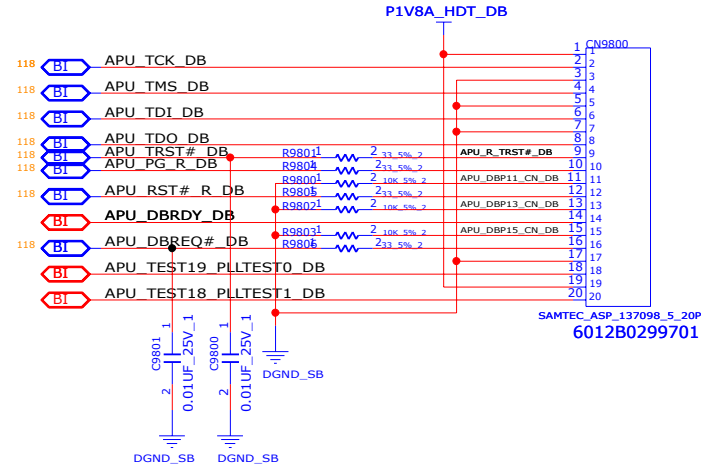
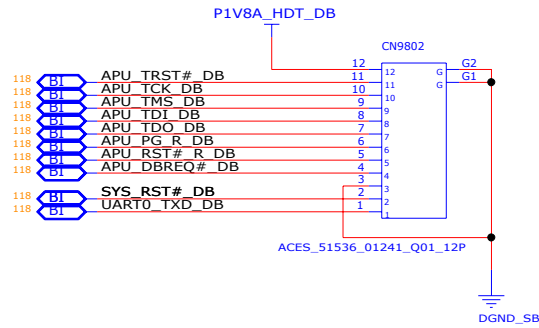
<https://realschematic.com>

INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by	DATE	PCB VER.	SHEET
XXX	21-OCT-2002	XXX	117 of 119
PCB P/N	60xxxxxxxxxx		

CHANGE by	DATE	PCB VER.	SHEET
XXX	21-OCT-2002	XXX	117 of 119
PCB P/N	60xxxxxxxxxx		

HDT DEBUG

LOCATION NUMBER : 9800~9849

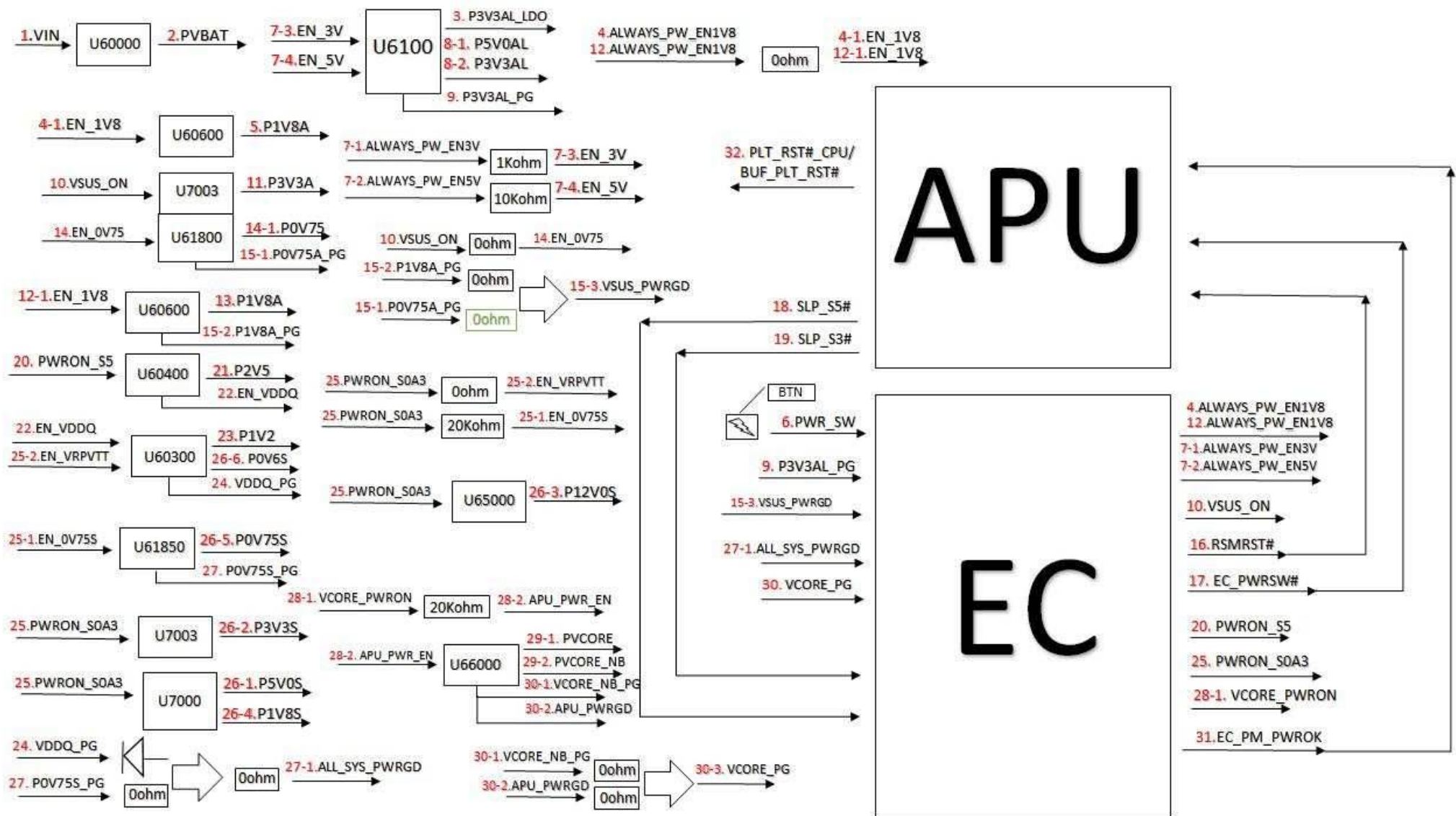


<https://realschematic.com>

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by		DATE	
PCB P/N		PCB VER	
XXX		21-OCT-2002	
60xxxxxxxxxxx		XXX	
SHEET		118 of 119	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxxx	PCB VER	XXX
SIZE	A3	CODE	CS
DOC.NUMBER	1310xxxxx-0-0	REV	X01
SHEET	118 of 119		



INVENTEC			
TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by		DATE	21-OCT-2002
PCB P/N		PCB VER	XXX
SHEET		119 of 119	